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Inversion-mode GaAs Wave-Shaped Field-Effect Transistor on GaAs (100) Substrate

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Inversion-mode GaAs wave-shaped metal-oxide-semiconductor field-effect transistors (WaveFETs) are demonstrated using atomic-layer epitaxy of La_2O_3 as gate dielectric on (111)A nano-facets formed on a GaAs (100) substrate. The wave-shaped nano-facets, which are desirable for the device on-state and off-state performance, are realized by lithographic patterning and anisotropic wet etching with optimized geometry. A well-behaved 1 μm gate length GaAs WaveFET shows a maximum drain current of 64 mA/mm, a subthreshold swing of 135 mV/dec, and an $I_{\text{ON}}/I_{\text{OFF}}$ ratio of greater than 10^7 .

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GaAs has been considered to replace Si in logic applications for decades due to its high electron mobility ^[1]. To achieve high on-current surface-channel inversion-mode n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) on GaAs (100) substrate is a long-time challenge. The main obstacle is the lack of high-quality, thermodynamically stable dielectric on GaAs that can match the device criteria as SiO₂ on Si such as a mid-gap interface trap density (D_{it}) around $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. During the past decades, tremendous efforts have been made to improve the oxide/GaAs interface with most of focus on different types of oxides and formation methods ^[2-10]. Recent work finds that the oxide/GaAs interface quality is strongly dependent on semiconductor surface orientations. GaAs MOSFETs fabricated on (111)A surface exhibit much higher on-state current (I_{ON}) than other surface-orientations such as (100) and (111)B even with the same atomic-layer-deposited (ALD) oxide ^[11]. More interestingly, much larger I_{ON} can be achieved on GaAs (111)A substrate with single crystalline La-based oxide dielectrics by atomic-layer-epitaxy (ALE) ^[12]. Mid-gap D_{it} or Fermi-level-pinning problem is significantly reduced with epitaxial La₂O₃ on GaAs (111)A surface ^[13,14], because the number of dangling bonds are dramatically reduced due to the nature of epitaxial oxide/semiconductor interface. However, GaAs (111)A substrate is technologically less important than the widely available GaAs (100) substrate, in particular, for the development of a manufacturable device technology.

In this letter, we demonstrate GaAs wave-shaped MOSFETs (WaveFETs) on a GaAs (100) substrate by nano-engineering to form ALE La₂O₃ on (111)A nano-facets. GaAs (111)A surface is achieved on a GaAs (100) substrate by the development of an

well-controlled anisotropic wet etching process. GaAs MOSFETs are formed on wave-shaped (111)A surface channels with epitaxial La_2O_3 as dielectric. But all devices are fabricated on GaAs (100) substrates. These devices have on-state current (I_{ON}) of 64 mA/mm and transconductance (g_m) of 32 mS/mm with sub-threshold swing (SS) around 135 mV/dec. This work opens a new route to realize high-performance GaAs MOSFETs on (100) substrates potentially. The process development and deep understanding of surface chemistry on these nano-facets could also be very important for the emerging 3D III-V devices. ^[15-23]

Figure 1(a) and 1(b) show the schematic view and cross-sectional view of a GaAs WaveFET in this work fabricated on a semi-insulating GaAs (100) substrate with an ALE high-k dielectric. The detailed process flow is described in Figure 2(a). An HF and H_2O_2 based anisotropic wet etching process ^[24] was applied to form the wave structure with Ti/Au as hard mask illustrated in Figure 2(b). MOSFET fabrication starts with 2-inch semi-insulating GaAs (100) substrates. As-received wafers were first degreased by acetone, methanol and isopropanol, then wave patterns were defined by electron beam lithography and Ti/Au were deposited by electron beam evaporator. After lift-off process, periodically patterned Ti/Au strip hard masks were formed as illustrated in Figure 2(b). Then, the wafers were dipped into HF (49%): H_2O_2 (30%) (10:129) based solution to form the wave-shaped channels. (111)A surface was obtained due to the anisotropic property of the wet etching process ^[25]. The realization of (111)A other than (111)B is further confirmed by the electrical properties of the fabricated devices since the Fermi level on (111)B is expected to be pinned ^[11]. After removal of Ti/Au hard mask by KI

solution, the wafers were dipped into buffered oxide etch (BOE) for 30s and then soaked in 10% $(\text{NH}_4)_2\text{S}$ for 15min for surface passivation. After deionized water rinse, the wafers were quickly transferred into ALD deposition chamber. 5 nm epitaxial La_2O_3 and 10 nm amorphous Al_2O_3 were then deposited by ALE/ALD. GaAs WaveFETs with 8 nm amorphous Al_2O_3 only as gate dielectric were also fabricated as the control sample. The epitaxial La_2O_3 thin films employed here were deposited from the precursors lanthanum tris($\text{N,N}'$ -diisopropylformamidinate) and H_2O at 385°C , while the amorphous Al_2O_3 oxide capping layer was deposited with precursors of trimethylaluminum (TMA) and H_2O at 300°C . The purpose of Al_2O_3 capping layer is to prevent the reaction between La_2O_3 and moisture in air and water during the process. Source and drain (S/D) regions were formed by a two-step Si implantation with dose of $1 \times 10^{14} \text{ cm}^{-2}$ at 30 keV and $1 \times 10^{14} \text{ cm}^{-2}$ at 80 keV, followed by an 850°C rapid thermal annealing (RTA) in N_2 for 15 s. S/D ohmic contact area was first defined by e-beam lithography, and then BCl_3/Ar inductively coupled plasma (ICP) dry etching was applied to remove the Al_2O_3 and HCl wet etching was applied to remove the La_2O_3 above metal contact area. GeNiAu contact was then formed followed by a 420°C RTA in N_2 for 15 s. Then, Ti/Au were deposited as gate electrodes and test pads. All patterns were defined by a Vistec UHR electron beam lithography system. The fabricated devices have gate lengths (L_g) of 1 μm , 2 μm and 4 μm .

The illustration of anisotropic wet etch process (HF and H_2O_2) is shown in Fig. 3. In this process, the wave patterned direction is critical. The wave structure has to be patterned along $(0\bar{1}1)$ other than (011) as shown in Figure 3(a). The effect of wave

pattern direction is shown by cross-sectional scanning electron microscopy (SEM) pictures in Figure 3(b) and 3(c). Hard mask strips were patterned along $(01\bar{1})$ in Figure 3(b) and along (011) in Figure 3(c). Clear (111) surface is shown in Figure 3(b) but irregular structures are formed if hard mask strips were patterned along (011) . Meanwhile, optimized W_{Fin} and W_{Gap} are also important to form compact wave structure with sharp corners so that the maximum channel width with $(111)\text{A}$ surface can be realized within the fixed channel pitch from the top. Figure 4(a) shows the transmission electron microscopy (TEM) picture of the cross section of the wave channel. A high-resolution TEM image of the epitaxial interface, taken from a sample with 5 nm La_2O_3 /10 nm Al_2O_3 as gate dielectric, is also shown in Figure 4(b). The lattice mismatch of La_2O_3 on GaAs $(111)\text{A}$ is $\sim 0.04\%$. It is evident that a flat and sharp interface is formed even on fabricated $(111)\text{A}$ nano-facet. It has been proved by C-V measurement that the epitaxial $\text{La}_2\text{O}_3/\text{GaAs}$ $(111)\text{A}$ interface exhibits D_{it} on the order of $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, which is far below the D_{it} level of traditional amorphous oxide on GaAs $(111)\text{A}$ surface.^[12,13] Figure 4(c) depicts the top view SEM image of one finished GaAs WaveFET with a gate length of 2 μm .

Well-behaved output, transfer and trans-conductance characteristics of a 1 μm -gate-length inversion-mode GaAs WaveFET are plotted in Figure 5, showing a maximum drain current ($I_{\text{D,max}}$) of 64 mA/mm at a gate bias (V_{GS}) of 4 V and a drain bias (V_{DS}) of 2 V, a maximum g_{m} of 32 mS/mm at $V_{\text{DS}} = 2 \text{ V}$ and threshold voltage (V_{T}) of 1.32 V. SS of $\sim 135 \text{ mV/dec}$ is obtained with an equivalent oxide thickness (EOT) of $\sim 6 \text{ nm}$, indicating a mid-gap interface trap density of $4.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ which is simply estimated from

equation $SS \sim 60 \times (1+qD_{it}/C_{ox})$ mV/dec. SS could be further improved by optimizing fabrication process and reducing EOT. It will also improve the extrinsic drain current and trans-conductance by reducing the EOT of the dielectric and improving interface quality. Devices with different gate length L_g (1, 2 and 4 μm) show similar SS and V_T (not shown), indicating these devices are weakly affected by short channel effects. It is also expected that these GaAs devices with a large bandgap and 3D wave structures must have better immunity to short channel effects. The GaAs WaveFET with epitaxial La_2O_3 demonstrated here has $I_{D,\text{max}}$ about $1,000 \times$ larger than that of the reference GaAs sample with amorphous Al_2O_3 dielectric (not shown) and about $10,000 \times$ larger than that of GaAs planar MOSFET on GaAs (100) substrate with amorphous Al_2O_3 ^[11]. GaAs planar MOSFETs on GaAs (100) substrate with La_2O_3 as gate dielectric were also fabricated. Without the special surface orientation to form (111) hexagonal template, poor quality La_2O_3 dielectric was formed on GaAs (100) surface showing a weak gate modulation and minuscule $I_{D,\text{max}}$. Figure 5(d) summarizes the effective gate length L_{eff} and the series resistance (R_{SD}) extracted by plotting R_{tot} versus L_g , where R_{tot} represents the total channel resistance measured from devices with various gate lengths under $V_{GS}-V_T$ from 1 to 2.5 V. R_{SD} is determined to be $1.62 \Omega\cdot\text{mm}$, which is reasonable for implanted S/D on GaAs and can be further reduced by optimizing the processes of ion implantation and activation during S/D contact fabrication. Contact resistance (R_C) of $0.27 \Omega\cdot\text{mm}$ is extracted from transmission line method. Two third of R_{SD} is from the access resistance between Ohmic contacts to the channel underneath the gate. ΔL , defined as the difference between the mask gate length L_g and L_{eff} , is estimated to be $\sim 0.36 \mu\text{m}$, due to

the lateral dopant diffusion caused by high-temperature activation and/or the lithographic misalignment.

In conclusion, by realizing (111)A nano-facets on (100) surface by anisotropic wet etching and a high-quality epitaxial $\text{La}_2\text{O}_3/\text{GaAs}$ (111)A interface by ALE, we demonstrate inversion-mode GaAs WaveFETs on GaAs (100) substrates with much larger drain currents than those formed on planar GaAs (100) surface using the same dielectric process. The work opens up a new way to improve the III-V device performance by nano-engineering semiconductor 3D structures and interfaces with high- k dielectric.

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Figure Captions

Figure 1 (a) Schematic and (b) Cross-sectional view of an inversion-mode GaAs (100) WaveFET with ALE La_2O_3 .

Figure 2 (a) Fabrication process flow for inversion-mode GaAs (100) WaveFET with ALE high-k La_2O_3 . (b) Illustration of wave channel formation by anisotropic wet etching. GaAs (111)A surface on these nano-facets is achieved by anisotropic wet etching of GaAs using HF solution.

Figure 3 (a) Schematic diagram of wave patterned orientation. (b) and (c) Cross-sectional SEM images of wave structures patterning along $(01\bar{1})$ and (011) orientations.

Figure 4 (a) Cross-sectional STEM image of GaAs WaveFET structure covered with La_2O_3 and Al_2O_3 . (b) HRTEM image of $\text{La}_2\text{O}_3/\text{GaAs}$ interface. Epitaxial La_2O_3 forms a flat and sharp interface on wave surface. (c) SEM image of a GaAs (100) WaveFET device top view with $L_g = 2\mu\text{m}$. Parallel wave structures are clearly shown as device channel.

Figure 5 (a) Output and (b) transfer (c) g_m characteristics of a GaAs WaveFET with $L_g = 1\mu\text{m}$. The device shows maximum drain current of 64 mA/mm, a subthreshold swing of 135 mV/dec, a peak trans-conductance of 32 mS/mm, and an $I_{\text{ON}}/I_{\text{OFF}}$ greater than 10^7 . (d) Measured total resistance versus different mask gate lengths as a function of gate bias. R_{SD} of $1.62\Omega\cdot\text{mm}$ and ΔL of $\sim 0.36\mu\text{m}$ are determined from the fitting lines.

- Ti/Au Gate
- 10nm Al_2O_3
- 5nm La_2O_3
- GaAs(100) substrate

(a)

◆ Semi-Insulating GaAs(100) Substrate

◆ **Wave Channel Formation**

<1> **Hard Mask Deposition (Ti/Au)**

<2> **Wave Channel Etching ($\text{HF}+\text{H}_2\text{O}_2$)**

<3> **Gold Removal (KI solution)**

◆ Gate Dielectric Deposition

(BOE 30s and $(\text{NH}_4)_2\text{S}$ Surface Passivation)

- 5nm La_2O_3 /10nm Al_2O_3

- 8nm Al_2O_3

◆ Si-Implantation

(Two-step: 30KeV/ $1 \times 10^{14} \text{cm}^{-2}$ /80KeV/ $1 \times 10^{14} \text{cm}^{-2}$)

◆ Dopant Activation (850°C, 15s in N_2)

◆ S/D Contact Formation

<1> Oxide Etching

(BCl_3/Ar Dry Etch for Al_2O_3 /HCl Wet Etch for La_2O_3)

<2> Metal Deposition (GeNiAu)

<3> Ohmic Anneal (420°C, 15s in N_2)

◆ Gate Electrode Formation (Ti/Au)

(b)