Variability Improvement by Interface Passivation and EOT Scaling of InGaAs Nanowire MOSFETs

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Variability Improvement by Interface Passivation and EOT Scaling of InGaAs Nanowire MOSFETs

Jiangjiang J. Gu, Student Member, IEEE, Xinwei Wang, Heng Wu, Roy G. Gordon, and Peide D. Ye, Fellow, IEEE

Abstract—High performance InGaAs gate-all-around (GAA) nanowire MOSFETs with channel length \((L_{NW})\) down to 20nm have been fabricated by integrating a higher-k \(\text{LaAlO}_3\)-based gate stack with an equivalent oxide thickness of 1.2nm. It is found that inserting an ultrathin (0.5nm) \(\text{Al}_2\text{O}_3\) interfacial layer between higher-k and InGaAs can significantly improve the interface quality and reduce device variation. As a result, a record low subthreshold swing of 63mV/dec has been demonstrated at sub-80nm \(L_{ch}\) for the first time, making InGaAs GAA nanowire devices a strong candidate for future low-power transistors.

Index Terms—Variability, MOSFET, InGaAs, nanowire.

I. INTRODUCTION

II-V compound semiconductors have recently been explored as alternative channel materials for future CMOS technologies [1]. \(\text{In}_x\text{Ga}_{1-x}\text{As}\) gate-all-around (GAA) nanowire MOSFETs fabricated using either bottom-up [2], [3] or top-down technology [4]–[6] are of particular interest due to their excellent electrostatic control. Although the improvement of on-state and off-state device metrics has been enabled by nanowire width \((W_{NW})\) scaling, the scalability of the devices in [4] is greatly limited by the large equivalent oxide thickness \((EOT)\) of 4.5nm. Aggressive \(EOT\) scaling is required to meet the stringent requirements on electrostatic control [5], [7], [8]. It is shown recently that sub-1nm \(EOT\) with good interface quality can be achieved by \(\text{Al}_2\text{O}_3\) passivation on planar InGaAs devices [9]. Considering the inherent 3D nature of the nanowire structure, whether such a gate stack technology can be successfully integrated in the InGaAs nanowire MOSFET fabrication process remains to be shown. In addition, the electron transport in the devices [4] can be enhanced by increasing the Indium concentration in the InGaAs nanowire channel, which promises further on-state metrics improvements such as on-current \((I_{ON})\) and transconductance \((g_m)\).

In this letter, we fabricated \(\text{In}_{0.65}\text{Ga}_{0.35}\text{As}\) GAA nanowire MOSFETs with atomic layer deposited (ALD) \(\text{LaAlO}_3\)-based gate stack \((EOT=1.2nm)\). ALD \(\text{LaAlO}_3\) is a promising gate dielectric for future 3D transistors because of its high dielectric constant \((k=16)\), precise thickness control, excellent uniformity and conformality [10]. The effect of ultra-thin \(\text{Al}_2\text{O}_3\) insertion on the device on-state and off-state characteristics has been systematically studied. It is shown that \(\text{Al}_2\text{O}_3\) insertion effectively passivates the \(\text{LaAlO}_3/\text{InGaAs}\) interface, leading to the improvement in both device scalability and variability. Record low subthreshold swing \((SS)\) of 63mV/dec has been achieved at sub-80nm \(L_{ch}\), indicating excellent interface quality and gate electrostatic control. Detailed device variation analysis has been presented for the first time for InGaAs MOSFETs, which helps identify new manufacturing challenges for future logic devices with high mobility channels.

II. EXPERIMENT

![Fig. 1. (a) Schematic diagram and (b) cross sectional view of InGaAs GAA nanowire MOSFETs with ALD \(\text{Al}_2\text{O}_3/\text{LaAlO}_3\) gate stack. (c) Output characteristics (source current) of InGaAs GAA nanowire MOSFETs \((L_{ch}=20nm)\) with \(\text{Al}_2\text{O}_3\)-first (solid line) and \(\text{LaAlO}_3\)-first (dashed line) gate stack.]

Fig. 1 (a) and (b) show the schematic diagram and cross sectional view of InGaAs GAA nanowire MOSFETs fabricated in this work. The fabrication process is similar to that described in [4]. A HCl-based wet etch process was used to release the InGaAs nanowires with minimum \(W_{NW}\) of 20nm. Each device had 4 nanowires in parallel as shown in Fig. 1(a). Because of the relatively high etch selectivity between InAlAs and InP, an additional 100nm InAlAs etch stop layer was added under the 80nm InP sacrificial layer to improve the control of the nanowire release process. The InGaAs nanowire channel consists of one 10nm \(\text{In}_{0.53}\text{Ga}_{0.47}\) layer sandwiched by two 10nm \(\text{In}_{0.65}\text{Ga}_{0.35}\) layers shown in Fig. 1(b), yielding a total nanowire height \((H_{NW})\) of 30nm. Here the heterostructure design ensures the high quality epitaxial layers grown by molecular beam epitaxy while maximizing the Indium concentration in the nanowire. A 0.5nm \(\text{Al}_2\text{O}_3\),
parasitic resistance, effective mobility and variation is impacted by several variation sources including variation by effective passivation of interface traps. The first devices, indicating a significant improvement in device statistical distribution of the on-state metrics, the box plots DIBL of 80mV/V and higher of 40mV/V, while the LaAlO$_3$ of 0.14V and 0.11V, respectively. For the off-state performance, in enhancement-mode, with a linearly extrapolated $V_T$ characteristics and used to calculate $g_m$. The Al$_2$O$_3$-first device shows higher $I_{ON} = 57 \mu A$/wire at $V_{DD} = V_{gs} = V_{gs} - V_T = 0.5V$ and peak transconductance $g_{m,max} = 165 \mu S$/wire at $V_{ds} = 0.5V$, compared to 48$\mu$A/wire and 155$\mu$S/wire for the LaAlO$_3$-first device. Both devices operate in enhancement-mode, with a linearly extrapolated $V_T$ of 0.14V and 0.11V, respectively. For the off-state performance, the Al$_2$O$_3$-first device shows a $SS$ of 75mV/dec and $DIBL$ of 40mV/V, while the LaAlO$_3$-first device shows higher $SS$ of 80mV/V and higher $DIBL$ of 73mV/V. To study the statistical distribution of the on-state metrics, the box plots for $I_{ON}$ and $g_{m,max}$ at $V_{DD} = 0.5V$ are shown in Fig. 3. The box plots include measurements from all 50 devices with $L_{ch}$ of 20nm and $W_{NW}$ of 20nm. Although only a 12% (10%) increase in mean $I_{ON}$ ($g_{m,max}$) is observed for the devices with Al$_2$O$_3$ insertion, a 54% (64%) reduction in standard deviation of $I_{ON}$ ($g_{m,max}$) is obtained on the Al$_2$O$_3$-first devices, indicating a significant improvement in device variation by effective passivation of interface traps. The $I_{ON}$ variation is impacted by several variation sources including parasitic resistance, effective mobility and $V_T$ variation [11], all of which are sensitive to the interface quality of the high-k/InGaAs nanowire surface.

To further investigate the scalability and off-state performance variability, the averages and standard deviations of $SS$, $DIBL$ and $V_T$ as a function of $L_{ch}$, are shown in Fig. 4 for Al$_2$O$_3$-first and LaAlO$_3$-first devices with $W_{NW} = 20nm$. The $SS$ and $DIBL$ remain almost constant with $L_{ch}$ scaling down to 50nm for both samples. This indicates that the current GAA structure with 1.2nm $EOT$ has yielded a very small geometric screening length and the devices show excellent resistance to short channel effects. Average $SS = 76$mV/dec and $DIBL = 25mV/V$ are obtained for Al$_2$O$_3$-first devices with $L_{ch}$ between 50 and 80nm, compared to 79mV/dec and 39mV/V for the LaAlO$_3$-first devices, indicating a reduction of interface trap density ($D_{it}$) with Al$_2$O$_3$ passivation. A small increase in $V_T$ is also observed for the Al$_2$O$_3$-first sample, which is ascribed to the reduction in negative donor-type charges at the interface. Furthermore, larger standard devia-
low interface quality of the LaAlO$_3$-first devices introduced additional device variation. It is also shown that the off-state performance variation increases as $L_{ch}$ scales below 50nm, which is ascribed to the reduction in electrostatic control.

![Fig. 5](image)

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