Variability Improvement by Interface Passivation and EOT Scaling of InGaAs Nanowire MOSFETs

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<td>Published Version</td>
<td>doi:10.1109/LED.2013.2248114</td>
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Variability Improvement by Interface Passivation and EOT Scaling of InGaAs Nanowire MOSFETs

Jiangjiang J. Gu, Student Member, IEEE, Xinwei Wang, Heng Wu, Roy G. Gordon, and Peide D. Ye, Fellow, IEEE

Abstract—High performance InGaAs gate-all-around (GAA) nanowire MOSFETs with channel length ($L_{ch}$) down to 20nm have been fabricated by integrating a higher-$k$ LaAlO$_3$-based gate stack with an equivalent oxide thickness of 1.2nm. It is found that inserting an ultrathin (0.5nm) Al$_2$O$_3$ interfacial layer between higher-$k$ and InGaAs can significantly improve the interface quality and reduce device variation. As a result, a record low subthreshold swing of 63mV/dec has been demonstrated at sub-80nm $L_{ch}$ for the first time, making InGaAs GAA nanowire devices a strong candidate for future low-power transistors.

Index Terms—Variability, MOSFET, InGaAs, nanowire.

I. INTRODUCTION

II-V compound semiconductors have recently been explored as alternative channel materials for future CMOS technologies [1]. In$_x$Ga$_{1-x}$As gate-all-around (GAA) nanowire MOSFETs fabricated using either bottom-up [2], [3] or top-down technology [4]–[6] are of particular interest due to their excellent electrostatic control. Although the improvement of on-state and off-state device metrics has been enabled by nanowire width ($W_{NW}$) scaling, the scalability of the devices in [4] is greatly limited by the large equivalent oxide thickness (EOT) of 4.5nm. Aggressive EOT scaling is required to meet the stringent requirements on electrostatic control [5], [7], [8]. It is shown recently that sub-1nm EOT with good interface quality can be achieved by Al$_2$O$_3$ passivation on planar InGaAs devices [9]. Considering the inherent 3D nature of the nanowire structure, whether such a gate stack technology can be successfully integrated in the InGaAs nanowire MOSFET fabrication process remains to be shown. In addition, the electron transport in the devices [4] can be enhanced by increasing the Indium concentration in the InGaAs nanowire channel, which promises further on-state metrics improvements such as on-current ($I_{ON}$) and transconductance ($g_{m}$).

In this letter, we fabricated In$_{0.65}$Ga$_{0.35}$As GAA nanowire MOSFETs with atomic layer deposited (ALD) LaAlO$_3$-based gate stack (EOT=1.2nm). ALD LaAlO$_3$ is a promising gate dielectric for future 3D transistors because of its high dielectric constant ($k=16$), precise thickness control, excellent uniformity and conformality [10]. The effect of ultra-thin Al$_2$O$_3$ insertion on the device on-state and off-state characteristics has been systematically studied. It is shown that Al$_2$O$_3$ insertion effectively passivates the LaAlO$_3$/InGaAs interface, leading to the improvement in both device scalability and variability. Record low subthreshold swing (SS) of 63mV/dec has been achieved at sub-80nm $L_{ch}$, indicating excellent interface quality and gate electrostatic control. Detailed device variation analysis has been presented for the first time for InGaAs MOSFETs, which helps identify new manufacturing challenges for future logic devices with high mobility channels.

Fig. 1(a) and (b) show the schematic diagram and cross sectional view of InGaAs GAA nanowire MOSFETs with ALD Al$_2$O$_3$/LaAlO$_3$ gate stack. (c) Output characteristics (source current) of InGaAs GAA nanowire MOSFETs ($L_{ch}$=20nm) with Al$_2$O$_3$-first (solid line) and LaAlO$_3$-first (dashed line) gate stack.

Manuscript received –. This work was supported in part by Air Force Office of Scientific Research (AFOSR) monitored by Prof. James C. M. Hwang and in part by Semiconductor Research Corporation (SRC) Focus Center Research Program (FCRP) Materials, Structures, and Devices (MSD) Focus Center. The review of this letter was arranged by Editor –.

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parasitic resistance, effective mobility and variation is impacted by several variation sources including variation by effective passivation of interface traps. The first devices, indicating a significant improvement in device performance, showed 3.12% (10%) increase in mean $I_L$ with $V_{DD} = 0.5V$. The box plots include measurements from all 50 devices for $I_{DIBL}$ of the Al$_2$O$_3$-first and LaAlO$_3$-first InGaAs GAA nanowire MOSFETs with $L_{ch} = 20nm$. The Al$_2$O$_3$-first device shows higher $I_{DIBL}$ of 73mV/V. To study the transfer characteristics and transconductance of the same MOSFETs with $L_{ch}$ scaling from 50 to 80nm, compared to 79mV/dec and 39mV/V for the LaAlO$_3$-first devices, indicating a reduction of interface trap density ($D_{it}$) with Al$_2$O$_3$ passivation. A small increase in $V_T$ is also observed for the Al$_2$O$_3$-first sample, which is ascribed to the reduction in negative donor-type charges at the interface. Furthermore, larger standard deviation of $SS$, $DIBL$ and $V_T$ and their standard deviations (STDs) for Al$_2$O$_3$-first and LaAlO$_3$-first InGaAs GAA nanowire MOSFETs with $W_{NW} = 20nm$.
low interface quality of the LaAlO$_3$-first devices introduced additional device variation. It is also shown that the off-state performance variation increases as $L_{ch}$ scales below 50nm, which is ascribed to the reduction in electrostatic control.

![Figure 5](image)

**Fig. 5.** (a) SS box plot and histogram for all Al$_2$O$_3$-first and LaAlO$_3$-first devices with $L_{ch}$ between 50–80nm and $W_{NW}$ of 20nm. (b) Transfer characteristic (source current) of a Al$_2$O$_3$-first and a LaAlO$_3$-first InGaAs GAA nanowire MOSFET with lowest SS of 63mV/dec and 69mV/dec, respectively.

Since these devices are immune to short channel effects, the first devices, indicating the effectiveness of Al$_2$O$_3$ passivation. The deviation and interquartile range has been obtained on Al$_2$O$_3$ and LaAlO$_3$ between 50$^\circ$C and 80$^\circ$C. The InGaAs GAA nanowire MOSFET is a promising candidate for low-power logic applications beyond 10nm.

**IV. Conclusion**

InGaAs GAA nanowire MOSFETs with $L_{ch}$ down to 20nm and $EOT$ down to 1.2nm have been demonstrated, showing excellent gate electrostatic control. The insertion of an ultra-thin 0.5nm Al$_2$O$_3$ between LaAlO$_3$/InGaAs interface has shown to effectively improve the scalability and variability of the devices. Near-60mV/dec SS is achieved on InGaAs nanowires with scaled $EOT$ and effective interface passivation. The InGaAs GAA nanowire MOSFET is a promising candidate for low-power logic applications beyond 10nm.

**ACKNOWLEDGMENT**

The authors would like to thank A. T. Neal, M. S. Lundstrom, D. A. Antoniadis, and J. A. del alamo for the valuable discussions.

**REFERENCES**


[3] K. Tomioka, M. Yoshimura, and T. Fukui, “Vertical In$_0.7$Ga$_0.3$As nanowire surrounding-gate transistors with high-k gate dielectric on Si substrate,” in *IEDM Tech. Dig.*, 2011, pp. 33.3.1–33.3.4.


