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La_{2-x}Sr_xCuO₄ Superconductor Nanowire Devices

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Abstract

La_{2-x}Sr_xCuO₄ nanowire devices have been fabricated and characterized using electrical transport measurements. Nanowires with widths down to 80 nm are patterned using high-resolution electron beam lithography. However, the narrowest nanowires show incomplete superconducting transitions with some residual resistance at T = 4 K. Here, we report on the refinement of the fabrication process to achieve narrower nanowire devices with complete superconducting transitions, opening the path to the study of novel physics arising from dimension-limited superconductivity on the nanoscale.

Keywords

La_{2-x}Sr_xCuO₄

Nanowire

Fabrication

ALL-MBE

Lithography

Critical current

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Introduction

Dimension-limited superconductivity on the nanoscale can provide insights into the fundamental underpinnings of high temperature superconductivity as well as having technological ramifications for novel device architectures. Recent applications of low-dimensional superconductor devices include single-photon detectors operating at quantum efficiency [1,2] and Josephson Junctions [3] as used in voltage standards. Nonetheless, important considerations arise on the nanoscale such as the fate of superconductivity as device dimensions shrink and approach the length scales of the magnetic penetration depth and superconducting coherence length [4].

Because of longer coherence lengths, which effectively set the scale for the dimensionality of superconductivity along the narrow length of the device, nanoscale devices fabricated from conventional low-temperature superconductors have been studied intensely for several decades. In particular, phase slips have been predicted and observed in nanowire devices of widths comparable to or smaller than the coherence length, i.e., in the quasi-1D limit [4-7]. These phase-slip events locally suppress the superconducting order parameter along a nanowire segment yielding a finite resistance even below the bulk critical temperature, T_c , and at low current bias smaller than the superconducting critical current, I_c . Although firmly established for low-temperature superconductors [7], observing phase slip processes arising from quantum fluctuations of the superconducting order parameter in cuprate superconductors remains an area of active investigation [8].

Fabricating nanowires from cuprate superconductors is advantageous because of higher T_c , higher j_c , and a larger superconducting energy gap. In previous studies, high- T_c wires were fabricated with widths ranging from micron-scale down to 10 nm [8-13]. Other nanostructures fabricated from high- T_c materials include nanorings and nano-loop networks probing magneto-resistance oscillations [14,15]. Interesting superconductivity effects reported in $\text{YBa}_2\text{Cu}_3\text{O}_7$ nanostructures include: thermally activated phase slips [9], very high j_c values close to the Ginzburg-Landau (GL) depairing limit [9,12], anomalous magnetoresistance oscillations in nanowires [10,11] and finally, telegraph noise in the pseudogap regime ascribed to stripe domain switching [13,16]. Few studies to test the

universality of these observed phenomena and their relation to the underlying mechanism of high- T_c superconductivity have been carried out using other cuprate materials [14,15].

While most earlier work has focused on $\text{YBa}_2\text{Cu}_3\text{O}_7$ nanowires, here we report on a recipe for fabrication and transport characterization of $\text{La}_{2-x}\text{Sr}_x\text{CuO}_4$ (LSCO) nanowires. LSCO is of particular interest by virtue of its simple structure as well as the opportunity to cover the entire doping phase diagram. The technical advances reported here may open the access to dimension-limited physics in LSCO.

Materials and Methods

LSCO films were synthesized using atomic-layer-by-layer molecular beam epitaxy (ALL-MBE), on $10 \times 10 \times 1 \text{ mm}^3$ LaSrAlO_4 (LSAO) substrates polished perpendicular to the (001) direction. The ALL-MBE growth technique allows for digital control of the LSCO film thickness, as reported previously in the synthesis of films showing interface superconductivity [17,18]. Reflection high-energy electron diffraction (RHEED) was used to monitor film crystallinity during growth. Strong diffraction streaks were observed without any transmission spots; together with pronounced oscillations in the intensity of the specular spot, this was an indication of atomically smooth interfaces and surfaces, without any secondary-phase precipitates. Atomic Force Microscopy (AFM) was used post-growth to characterize the surface roughness of LSCO films. Typical values of rms surface roughness observed by AFM with a $9 \mu\text{m}^2$ scan area were in the range of 2-3 Å as seen in Fig. 1a. Films patterned in this study had compositions in the underdoped region ($\text{La}_{1.89}\text{Sr}_{0.11}\text{CuO}_4$ and $\text{La}_{1.90}\text{Sr}_{0.10}\text{CuO}_4$) and at the optimal doping level ($\text{La}_{1.84}\text{Sr}_{0.16}\text{CuO}_4$). For each film, the surface was protected by a 10 nm thick capping gold layer, deposited *in situ*. Mutual inductance measurements of the sample susceptibility were carried out to determine the film's bulk T_c before lithographic patterning. Fig. 1b shows typical mutual inductance data.

Four-point-contact nanowire devices were fabricated using high-resolution electron-beam lithography (EBL). The negative-tone MA-N240x resist was spun to a thickness ranging between 100 nm and 400 nm (Fig. 2a) and exposed in an electron beam writer. Two writers, a JEOL 6300FS and an FEI Helios dual beam NPGS, were used for EBL patterning with accelerating voltages of 10 kV - 30 kV

and 100 kV, respectively. Beam currents 25 pA – 500 pA were used to write nano-features ranging from 80 nm to 2 μm widths, while the large contact-pad patterns were exposed using larger currents, between 1 nA and 4 nA, with EBL accelerating voltage-dependent beam doses of 50 – 120 $\mu\text{C}/\text{cm}^2$. In the areas exposed to the electron-beam flux the resist cross-links, and becomes resilient to the developer. Unexposed regions are washed away by the developer solution (Fig. 2b). The cross-linked negative-tone resist pattern serves as an etch mask in a subsequent pattern transfer step.

The pattern was transferred into the LSCO film and down to the LSAO substrate using an Ar^+ ion milling process, with 350 V – 1 kV beam voltage and 25-50 mA beam current, using a 2-inch ion source (Fig. 2c). Films were ion-milled on either a liquid-nitrogen-cooled or a water-cooled stage to mitigate sample damage during the ion milling procedure. For devices whose intrinsic properties we intended to characterize above T_c , a second EBL step was performed to remove the Au-capping layer. For the second EBL, we used alignment marks defined in the first EBL exposure to open up a window in the positive PMMA resist only atop a segment of the nanowire. A quick etching step was used to remove the Au-shorts, thus allowing for measurements of the bare LSCO devices (Fig. 2d).

We used a scanning electron microscope (SEM) to image nanowire devices, and measure their line widths. Figures 3a and 3b show a typical Au-capped single nanowire device where the current source-drain and voltage leads are made of the same LSCO film as the nanowire in order to avoid contact-resistance issues that sometime arise for interfaces between high- T_c superconductors and common metals. In Fig. 3b, a voltage drop is measured across a nanowire segment of length 2.5 μm . The device seen in Fig. 3a and in Fig. 3b is still protected by a negative-tone resist etch mask, with brighter regions indicating the etched LSAO substrate. Bare LSCO nanowire devices (stripped of the protective Au over layer) were fabricated and imaged by SEM, as well. A representative bare LSCO nanowire device, 90 nm wide and with voltage measured across a nanowire segment of 500 nm, is shown in Fig. 3c.

Electrical transport characterization of LSCO nanowire devices was carried out using a home-made variable-temperature (4 K to 300 K) cryostat, using a low-noise four-terminal configuration method. Resistance versus temperature, $R(T)$,

and current-voltage (I - V) characteristics were measured for the fabricated nanowire devices using a DC current-bias technique. I - V measurements were used to measure I_c for superconducting nanowires below the superconducting transition temperature. Low-current-bias conditions, below the device I_c , were used for $R(T)$ measurements.

While here we report only the results of four-point resistance measurements on single nanowires, we have also fabricated and studied various nanowire-array devices containing up to 10 nanowires in parallel.

Results and Discussion

Hundreds of nanowires were fabricated and measured in this study. For each nanowire, the sudden drop in measured $R(T)$ occurred at essentially the same T_c as the value measured by mutual inductance technique in the same film before it was patterned. In nanowires patterned out of underdoped LSCO films with the nominal doping level $x = 0.11$ and $x = 0.10$, we measured abrupt resistance drops at 19 K, comparable to the bulk value of T_c . An obvious problem that arose for this fabrication process, as observed by electrical transport measurements, was the presence of a residual resistance in $R(T)$ curves even at $T = 4$ K, as seen in Fig. 4. Consistent with this finding was the absence of critical current in the I - V characteristics. Such incomplete resistive superconducting transitions were observed in the majority of devices measured. Residual resistance values varied from 10 m Ω to 10 k Ω , while our resistance measurement resolution was better than 1 m Ω . Lower residual resistance values were generally found in wider, optimally doped, Au-capped LSCO nanowire devices, while higher residual values were typically seen in narrower, underdoped, bare nanowire devices.

In principle, incomplete superconducting resistive transitions could arise intrinsically as a result of phase-slip processes. However, we rule out this explanation, because the nanowires were up to two-orders-of-magnitude wider than the coherence length - the scale where such behavior is usually observed. Moreover, the resistive transitions were not broadened enough to fit the exponential $R(T)$ dependence expected from the widely accepted Langer-Ambegaokar-McCumber-Halperin (LAMH) theory of thermally activated phase slips (TAPS) [19,20].

Therefore, we surmise that the primary causes of the residual resistance in our nanowire devices are extrinsic factors such as electron-beam damage, ion-beam damage during Ar^+ milling, or both. Electron irradiation was previously observed to introduce defects in cuprates [21], so electron beam-induced defects may be a likely culprit. In Table 1, we compare the values of residual resistance in several bare LSCO nanowire devices that were exposed to an electron beam during SEM characterization, with others that were not exposed. From Table 1, we observe an overall correlation between devices exposed to the SEM and higher residual resistances subsequently measured for those devices. In subsequent fabrication of nanowire devices, we used lower electron-beam accelerating voltage, and lower electron beam doses administered to the negative-tone resist, yet this failed to consistently produce nanowire devices with complete superconducting transitions.

Consequently, we modified the ion-milling step to be less invasive. We scaled the beam voltage down from 500 V – 1 kV to 350 V, and the beam current from 50 mA down to 25 mA, the values just barely sufficient to ignite and sustain the Ar^+ -ion milling plasma. In addition, during the ion-milling process, we cooled the sample holder by liquid nitrogen, in order to minimize possible oxygen loss from the LSCO film. For the optimally doped LSCO films with reduced beam voltage and beam current during ion milling, we observed an improvement in the nanowire device properties.

In Fig. 5a, we show complete superconducting resistive transitions observed in Au-capped LSCO nanowires of varying widths, fabricated on the same film. The normal-state resistance generally gets higher the narrower the wire is, except for the 500 nm wide wire where we suspect a local substrate defect or scratch could have increased the measured resistance. The onset critical temperature in Fig. 5a, taken to be the temperature where the resistance versus temperature curve deviates from linearity, shows a weak dependence on the nanowire width. The wires shown in Fig. 5a all show onset critical temperatures within 2.5 K of each other, with no clear and systematic dependence on the wire width. Upon analyzing for each wire the temperature value where the wire resistance vanishes, and fitting to a linear regression versus the wire width, we find a trend: wider wires achieve the zero resistance state at higher temperatures. The widest 2 μm wire shows complete superconductivity at 9 K higher temperature than the 350 nm wide nanowire.

Furthermore, we observe a trend that the superconducting resistance transition gets narrower as the wires become wider. Together, the above insights indicate that extrinsic damage from the lithographic process pipeline has a stronger role in limiting superconductivity for narrower structures than for wider wires.

Fig. 5b shows the corresponding values of current density for the same set of LSCO devices as in Fig. 5a, with critical current densities reaching $j_c \approx 10^8$ A/cm². No clear trend is observed in the dependence of the wire critical current density on the wire width. The observed high critical current densities might indicate the presence of flux pinning centers in the sample most likely introduced during the sample patterning process.

Such high critical current density values for Au-capped nanowire devices with complete superconducting transitions indicate how critical the ion-milling step can be in the patterning of nanowire devices in cuprates, particularly in LSCO. With all the listed precautions to mitigate the damage from the ion-milling process, we have fabricated nanowire 4-terminal devices down to 300 nm wide, with complete superconducting transitions. The critical role of the ion-milling step has been suggested also by other groups working with YBCO films [22].

Conclusions

We have grown LSCO films on LSAO substrates by ALL-MBE, and patterned them into four-terminal nanowire devices, with widths down to 80 nm. The critical technical hurdle was that nanowires tended to show non-zero residual resistance and incomplete superconducting transitions. These residual resistances limited the minimal width of superconducting nanowire devices that could be fabricated using this recipe. We tracked the underlying cause of the incomplete superconducting transition to the sensitivity of cuprate films to damage by electron and ion beams, to which they were exposed in the nanowire fabrication process. We took additional measures, particularly during ion-milling, to minimize the film damage during these process steps, such as utilizing liquid-nitrogen cooling of the sample stage and reduction of the ion milling beam voltages and current. Subsequently, we observed complete superconducting transitions in nanowire down to 300 nm wide. Further work, using non-invasive lithographic techniques for patterning even narrower LSCO nanowires, is in progress. By continuing to trim down the width of

LSCO nanowire devices, we hope to access novel physics arising from dimension-limited superconductivity on length scales smaller than the penetration depth and comparable to the coherence lengths in these cuprate materials.

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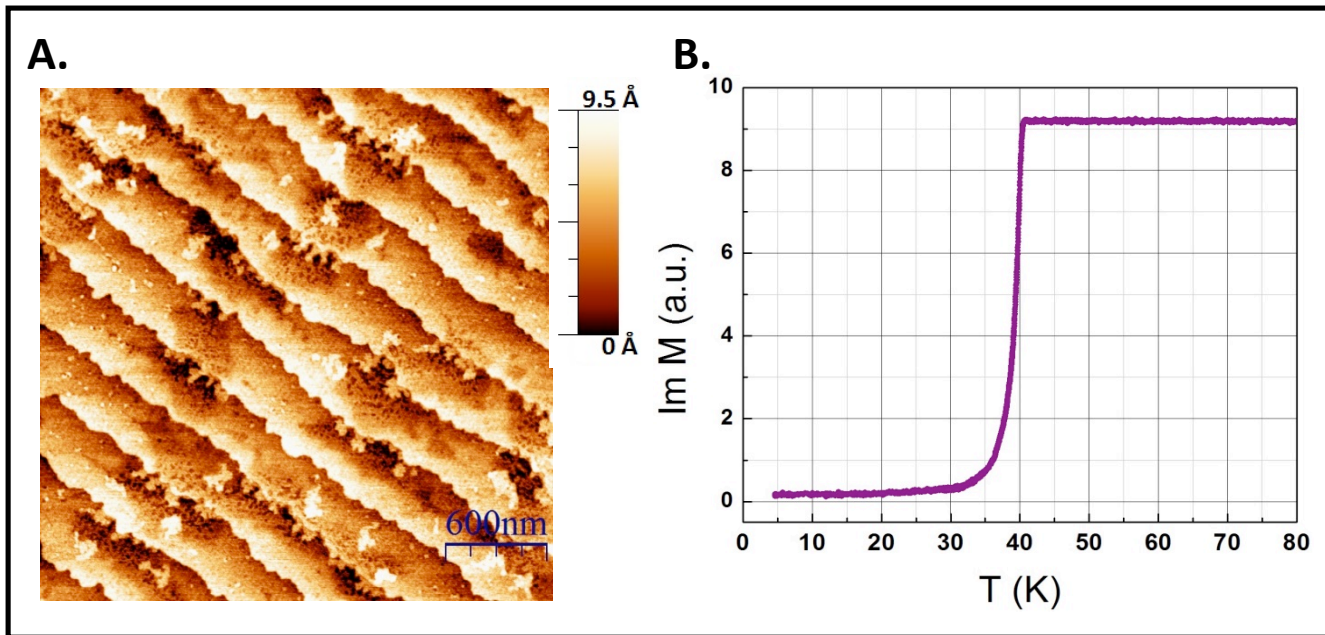


Fig. 1: Typical AFM and mutual inductance data of LSCO films.

A) An AFM image of an ALL-MBE-grown LSCO film, showing the rms surface roughness less than 3 \AA , over a 9 \mu m^2 scan area.

B) The imaginary part of the mutual inductance of an optimally doped, 20 unit cell thick LSCO film, showing $T_c = 41 \text{ K}$.

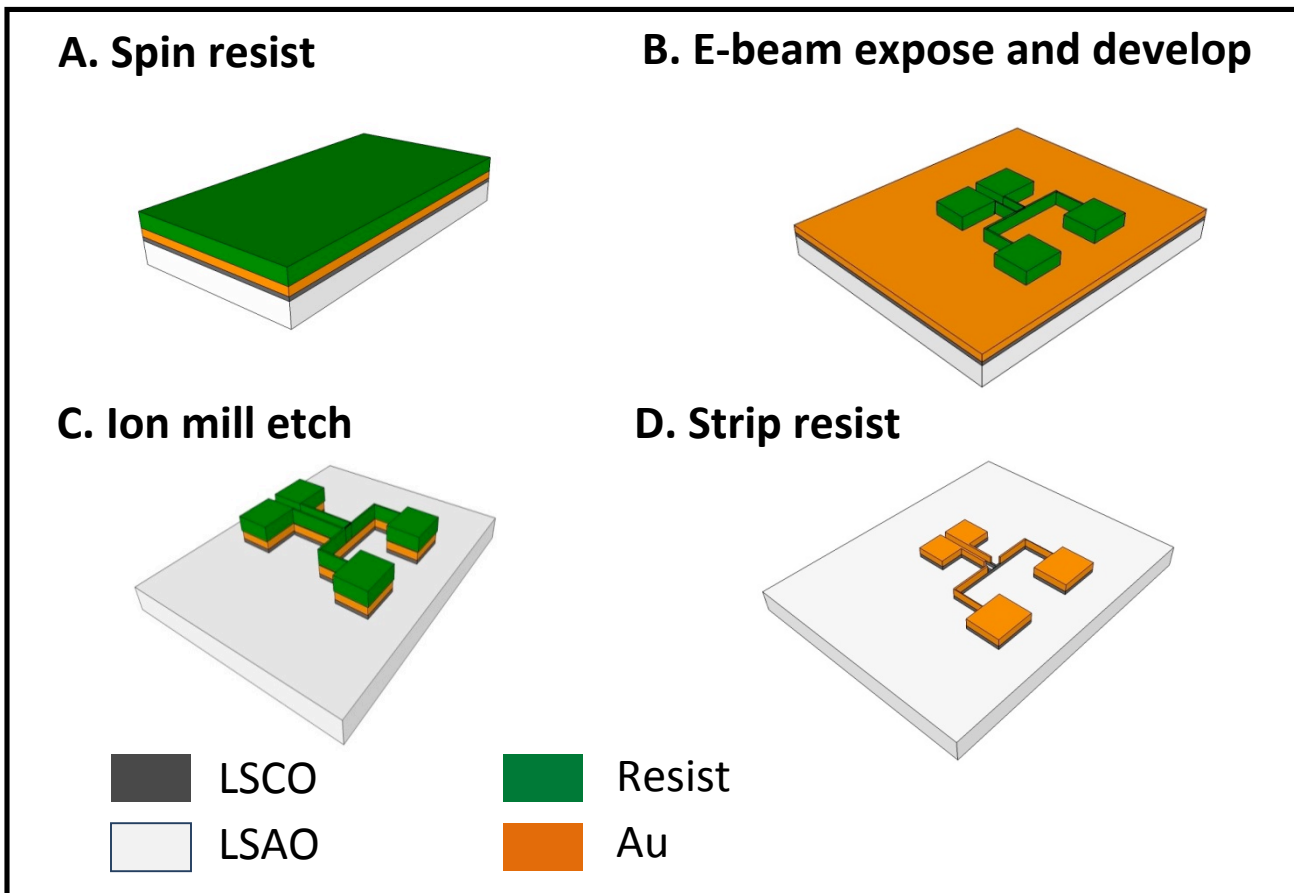


Fig. 2: Fabrication recipe for LSCO nanowire devices.

A) Electron (e-) beam resist was spun on a Au-capped sample.

B) The resist was exposed with an e-beam, and developed.

C) Pattern transfer was carried out using Ar^+ ion milling.

D) The e-beam resist was stripped off, producing the final LSCO nanowire device.

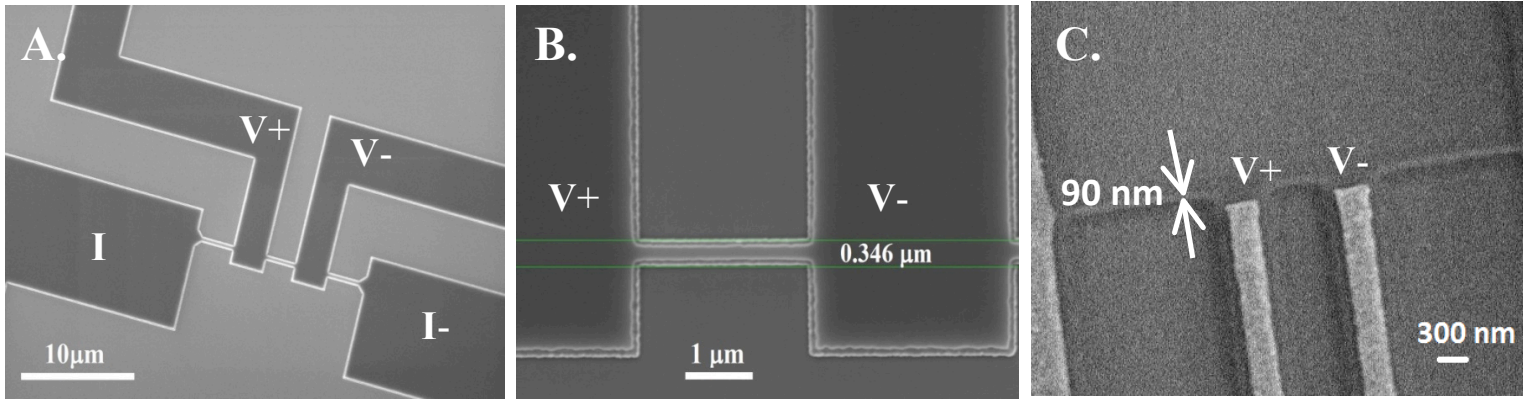


Fig. 3: SEM images of LSCO nanowire devices.

A) LSCO nanowire device (dark areas) after pattern transfer down to the LSAO substrate (lighter areas), capped with a protective Au layer and electron beam resist. Current source-drain and voltage leads are as indicated.

B) A zoom of the same LSCO device, with voltage leads visible and separated by $2.5 \mu\text{m}$.

C) A bare LSCO nanowire device of width 90 nm . The voltage leads, separated by 500 nm , are the two lighter regions at the center of the image.

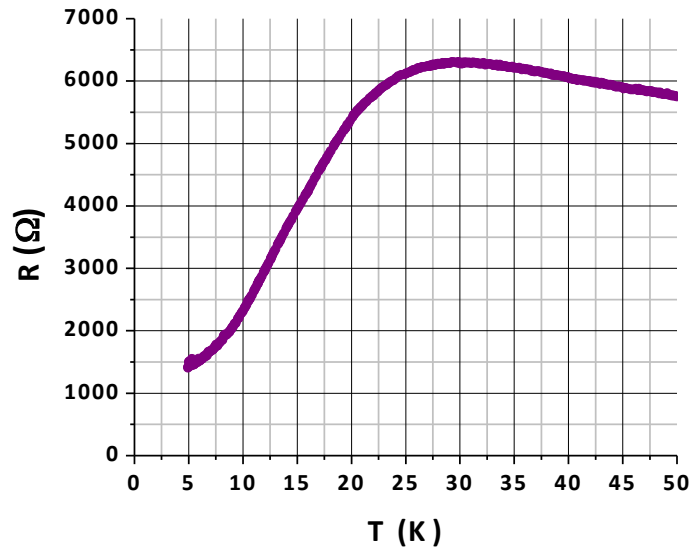


Fig. 4: Temperature dependence of resistance in a 170 nm-wide nanowire fabricated out of an underdoped LSCO film. A current bias of 4 nA was used for the resistance measurement. The resistive transition is incomplete, showing a high residual resistance, larger than 1 k Ω .

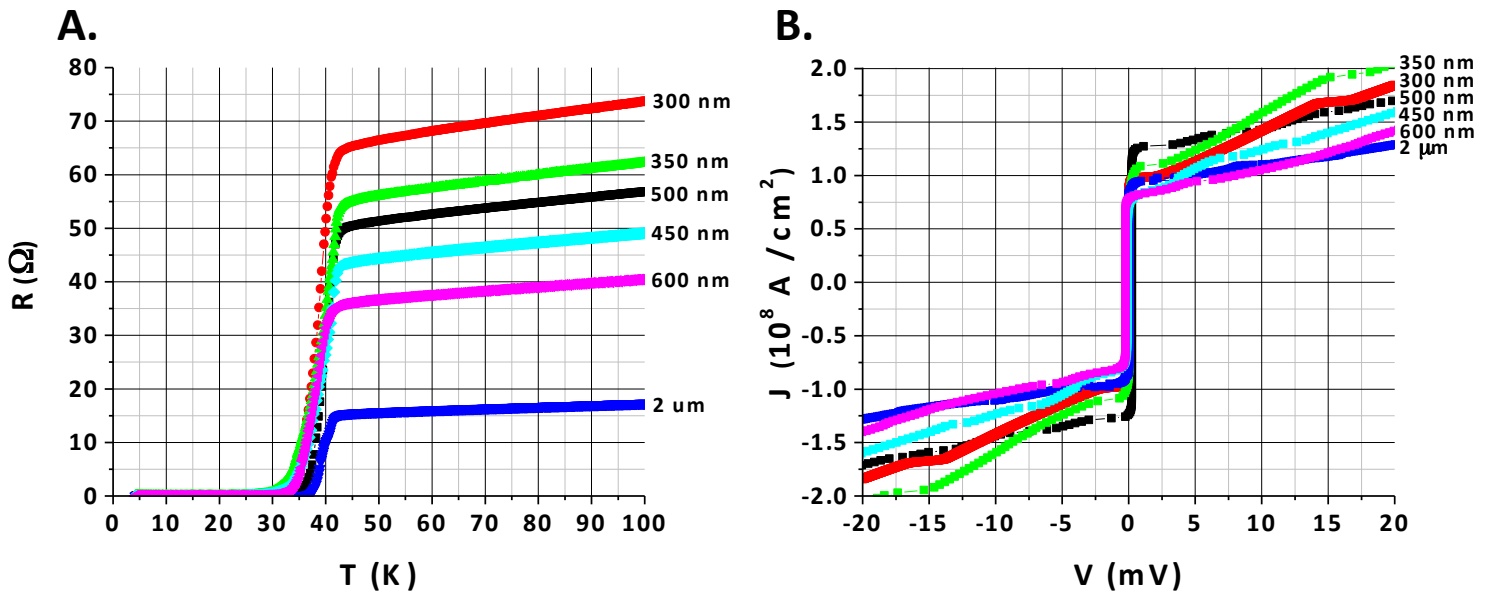


Fig. 5: $R(T)$ and $I-V$ characteristics of six devices of varying width, all fabricated on the same optimally-doped LSCO film for easier comparison. The pattern transfer was carried out using a reduced beam voltage (350 V) and current (25 mA) during the ion milling step.

A) Every measured device fabricated from the same LSCO film shows a complete superconducting transition. The resistance was measured with a current bias of 1 μA .

B) The same devices show high critical current values, up to 10^8 A/cm^2 .

Device #	1	2	3	4	5	6	7	8	9	10	11	12
Width (nm)	80	80	140	140	180	200	200	200	200	250	300	300
R (Ω/\square)	156	556	OL	OL	3.4	7	15	120	350	1.8	2.7	2.7
SEM exposed	Yes	Yes	Yes	Yes	No	Yes	No	No	Yes	No	No	No

Table 1. The effect on the residual resistance of a nanowire exposed to a 5 kV SEM electron beam. OL = overload, i.e., resistance $> 1 \text{ G}\Omega$. For best comparison, all the measured devices fabricated from the same LSCO film are listed here.