A fully integrated battery-connected switched-capacitor 4:1 voltage regulator with 70% peak efficiency using bottom-plate charge recycling

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A Fully Integrated Battery-Connected Switched-Capacitor 4:1 Voltage Regulator with 70% Peak Efficiency Using Bottom-Plate Charge Recycling

Tao Tong, Xuan Zhang, Wonyoung Kim, David Brooks, Gu-Yeon Wei
School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, U.S.A
E-mail: taotong@seas.harvard.edu

Abstract—This work presents a switched-capacitor (SC) DC-DC voltage regulator that converts a 3.7V battery voltage down to ~0.8V in order to power the ‘brain’ SoC of a flapping-wing microrobotic bee. A cascade of two 2:1 SC converters offers high efficiency for a 4:1 conversion ratio. A charge recycling technique reduces the flying capacitor’s bottom-plate parasitic loss by 50% and overall conversion efficiency reaches 70%. The output droop is less than 10% of the nominal output voltage for a worst-case 47mA load step.

I. INTRODUCTION

In the aerial microrobotic bee application [1], the on-board battery (~3.7V) is the only source of energy. A digital SoC, which works as the ‘brain’ of the robotic bee, operates at low voltages (~0.8V or less). While a voltage regulator is required to bridge the voltage difference, the stringent weight and area requirements of the robotic bee make the regulator design challenging. First, the regulator needs to be fully integrated along with the SoC without using any external components in order to minimize weight and area. Second, the regulator must directly connect to the battery and support a high (4:1) step down ratio. Third, high conversion efficiency is important to achieve long flight times for the robotic bee.

SC converters are well suited for this application from weight and area perspectives since they only require capacitors and MOS transistors. On-chip MOS capacitors with density as high as 10nF/mm² are available in digital CMOS processes [2]. However, choosing the right topology is important. Single-stage SC converters suffer from power switch voltage breakdown and high bottom-plate parasitic loss when the conversion ratio and input voltage are high [2][4][5]. One solution has been to cascade thick-oxide transistors to avoid transistor break down in 3:1 SC converters [2][5], but this degrades conversion efficiency. Novel switching techniques have also been shown to mitigate flying capacitor bottom-plate parasitic loss [4][8]. Unfortunately, these issues get worse in single-stage 4:1 SC converters.

This paper presents a fully integrated two-stage SC regulator to address these challenges. The proposed two-stage topology simplifies the overall design and implements several techniques to improve conversion efficiency: (1) it uses the appropriate flavor of transistors (thin oxide and think-oxide transistors) in each stage; (2) it applies a charge recycling technique to mitigate bottom-plate parasitic loss; and (3) it employs separate low-boundary feedback controls to regulate the each stage’s output to desired levels. Lastly, the two-stage topology provides an intermediate voltage for use by other parts of the microrobotic bee.

II. PROPOSED TWO-STAGE CONVERTER

A. Two-Stage Structure

Fig. 1 illustrates the system block diagram of the proposed SC converter. The design cascades two 2:1 SC stages, which are implemented and optimized for different purposes. The first stage converts the 3.7V battery voltage down to a 1.8V intermediate voltage (V\textsubscript{INT}). To handle the 1.8V swing, this stage uses thick-oxide transistors available in the process. The second stage converts the intermediate 1.8V down to ~0.8V for the final output (V\textsubscript{OUT}) using thin-oxide transistors. Each stage also includes identical, but separate feedback control loops, discussed later.

The two SC stages are nearly identical except for the type of transistors and sizing. Each SC stage implements a multi-phase topology to reduce voltage ripple. Sixteen modules operate off both edges of eight interleaved clock phases. A multi-phase current-starved pseudo-differential VCO generates the clock edges and operates directly off of the battery to guarantee proper start-up. To ensure there is always a balanced number of modules in operation, pairs of modules operate 180° out-of-phase off of one shared clock phase. SC converters have two basic phases of operation, thoroughly discussed in [2]. In one phase, energy drawn from the input charges the flying capacitor up and flows to the load. In the other phase, energy stored on the capacitor during the previous phase flows to the load. The power switches operate with stacked voltage domains similar to [3] and [6]. Taking the first-stage as an example, switches driven by S\textsubscript{1L} and S\textsubscript{1H} operate in the high voltage domain (between V\textsubscript{INT} and V\textsubscript{BAT}) while switches driven by S\textsubscript{2L} and S\textsubscript{2H} operate in the low voltage domain (between ground and V\textsubscript{INT}).

The maximum switching frequencies of the two stages are also different. The first-stage maximum switching frequency is one quarter of that in the second stage. By doing this, the two stages occupy similar chip area and have similar conversion efficiencies, resulting in optimal overall efficiency and power density for the regulator. By optimizing the two stages separately, the first stage connects to the high battery voltage.
but is decoupled from output load transients. The higher switching frequency of the second stage enables higher closed-loop bandwidth for fast output load transient response.

Cascading two 2:1 SC stages offers other advantages. $V_{\text{OUT}}$ and $V_{\text{OUT}}$ can serve as stacked supply voltages for the switch drivers in each stage such that no additional voltage rail is required. Also, the bottom plate parasitic loss is lower, compared to single-stage 4:1 SC converters, which we further reduce via a charge recycling technique described below.

### B. Bottom-Plate Charge Recycling

A dominant source of efficiency loss in SC converters comes from switching the bottom-plate parasitic capacitance associated with the flying capacitor ($C_{\text{FLY}}$). All of the flying capacitors in this design rely on bulk MOS transistors, which usually have non-negligible bottom-plate parasitic capacitance (~2% in this technology, ~5% in [4]). Each stage implements a circuitry that combines two-step charging/discharging with charge recycling, as illustrated in Fig. 2 for the second stage. $C_{\text{PAR}}$ is the parasitic bottom-plate capacitor of $C_{\text{FLY}}$. By adding an additional recycling capacitor, $C_{\text{REC}}$, the proposed technique avoids using an external voltage source. The two-step charging/discharging occurs during the converter’s dead time to recycle charge, reduce losses, and improve conversion efficiency.

The charge recycling operation is as follows. Assume $C_{\text{REC}} \gg C_{\text{PAR}}$, and $V_{\text{REC}}$ starts out at $V_{\text{OUT}}/2$. When discharging $C_{\text{PAR}}$, $C_{\text{PAR}}$ first transfers charge to $C_{\text{REC}}$ through the additional switch controlled by $\Phi_{\text{REC}}$. In this process, $C_{\text{PAR}}$ discharges from $V_{\text{OUT}}$ to $V_{\text{OUT}}/2$. Then, the switch $\Phi_{\text{REC}}$ turns off and $C_{\text{PAR}}$ fully discharges to ground. The amount of charge transferred from $C_{\text{PAR}}$ to $C_{\text{REC}}$ is $C_{\text{PAR}}V_{\text{OUT}}/2$, which is stored on $C_{\text{REC}}$ and is recycled in the charging phase. When charging $C_{\text{PAR}}$, $C_{\text{PAR}}$ first charges up from ground to $V_{\text{OUT}}/2$ via $C_{\text{REC}}$. In this period, $C_{\text{REC}}$ transfers $Q=C_{\text{PAR}}V_{\text{OUT}}/2$ to $C_{\text{PAR}}$, which is the same amount of charge that $C_{\text{REC}}$ gets from $C_{\text{PAR}}$ in the discharging process. $C_{\text{PAR}}$ then disconnects from $C_{\text{REC}}$ and fully charges up to $V_{\text{OUT}}$. From an energy perspective, $V_{\text{OUT}}$ only needs to provide $E=C_{\text{PAR}}V_{\text{OUT}}^2/2$ in this charging process, which is half of the energy otherwise required. It is important to note that $V_{\text{REC}}$ eventually settles to $V_{\text{OUT}}/2$ regardless of its initial voltage, because this is the only balanced state where the energy stored on $C_{\text{REC}}$ when discharging $C_{\text{PAR}}$ matches the energy that $C_{\text{REC}}$ loses when charging $C_{\text{PAR}}$.

The above recycling process assumes $C_{\text{REC}} \gg C_{\text{PAR}}$. Thanks to the converter’s multi-phase operation, $C_{\text{REC}}$ can be shared by all of the phases and $C_{\text{REC}}$ only needs to be larger than the parasitic capacitance in one phase, achieved with negligible penalty. In this implementation, $C_{\text{REC}}$ is 2% of the total flying capacitance.
VOUT and POUT. The transient responses in open- and closed-loop operation are discussed in Section III.C. Finally, Section D provides a summary of test chip characteristics and compares it to prior work.

A. Voltage ripple

This section presents the experimentally measured results as follows: Section III.A first compares steady-state voltage ripple for open- and closed-loop modes of operation. Then, Section III.B presents conversion efficiency results versus VOUT and POUT. The transient responses in open- and closed-loop modes of operation are discussed in Section III.C. Finally, Section D provides a summary of test chip characteristics and compares it to prior work.

B. Conversion efficiency

In SC converters, the major sources of efficiency loss are...
a 3mA to 50mA load step causes VOUT to drop by ~100mV.

The converter runs in open-loop with maximum switching frequency and ~100ps rise and fall times. As seen in Fig. 9(a), when the SC converter runs in open-loop with maximum switching frequency, a 3mA to 50mA load step causes VOUT to drop by ~100mV. When running in closed-loop with the nominal output voltage set to 750mV, however, the control loop quickly reacts and the voltage droop caused by the load current step is much smaller. In fact, the ~60mV droop in Fig. 9(c) is mostly due to the larger steady-state voltage ripple previously seen with respect to higher output power.

**D. Test chip summary**

The silicon area, shown by the micrograph in Fig. 10, was not optimized for power density but was governed by the pads and circuitry added for testing. Flying capacitors and output filter capacitors, which occupy half of the overall area, total 2.64nF. Table 1 compares this work to prior art SC converters. The 70% peak efficiency of this design is comparable to the efficiencies in [3] and [5], but for a higher 4:1 conversion ratio.

**Fig. 9: Transient response (a) open-loop with maximum FSW, (b) closed-loop, and (c) zoom-in of (b)**

**Fig. 10: Die Photo**

**Table. 1 Comparison to prior art.**

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<th>CPT</th>
<th>Efficiency (%)</th>
<th>Peak eff.</th>
<th>Conversion ratio</th>
<th>Power density (mWh/mW@f)</th>
<th>Load step (mAh/mW@f)</th>
<th>Output droop</th>
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<td>74.3%</td>
<td>3.1</td>
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<td>41.7@50ps</td>
<td>76mV</td>
<td>[1]</td>
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<tr>
<td>[6]</td>
<td>90nm</td>
<td>3fF</td>
<td>74%</td>
<td>77%</td>
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<td>313</td>
<td>5.8@25ns</td>
<td>30mV</td>
<td>[2]</td>
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<td>66%</td>
<td>70%</td>
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<td>4,133</td>
<td>17.8@100ps</td>
<td>60mV</td>
<td>[7]</td>
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**IV. CONCLUSIONS**

This paper demonstrates a fully integrated battery-connected switched capacitor converter for the brain SoC of a microbotic bee. The two-stage topology, with bottom-plate charge recycling, offers high conversion efficiency for the high 4:1 conversion ratio. While closed-loop regulation provides fast transient response, it also exhibits larger steady-state voltage ripple, which results in efficiency drop compared to open-loop operation. This tradeoff motivates exploring an adaptive clocking strategy to improve overall system efficiency as described in [7].

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**REFERENCES**