AlGaN/GaN MOSHEMT on Si Substrate with High on/off Ratio and High Off-state Breakdown Voltage Enabled by Atomic Layer Epitaxial MgCaO as Gate Dielectric

Citation

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AlGaN/GaN MOSHEMT on Si Substrate with High on/off Ratio and High Off-state Breakdown Voltage Enabled by Atomic Layer Epitaxial MgCaO as Gate Dielectric

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AlGaN/GaN high-electron-mobility-transistors (HEMTs) on Si substrates have attracted more and more attention in the area of high voltage power switches due to their lower-cost substrates, large substrate diameters and their ability to integrate with silicon processes [1-3]. Conventional Schottky gate HEMTs suffer from relatively high gate leakage currents which limit maximum forward gate bias swing and off-state performance. Metal-oxide-semiconductor HEMTs (MOSHEMTs) are proposed with a thin oxide layer in between gate and barrier to solve the aforementioned problems [4]. A good oxide must have a sufficiently large barrier height and high interface quality. In this work, we incorporate epitaxial $Mg_{0.25}Ca_{0.75}O$ gate dielectric deposited by atomic layer deposition (ALD) into the GaN MOSHEMT process yielding improved device performance.

Fig. 1 shows schematic view of an AlGaN/GaN MOSHEMT on a Si (111) substrate with sheet resistance (R_{sh}) ~ 450 Ω/□. Device fabrication started with mesa isolation by Cl_2/BCl_3 etching to a depth of 150 nm. Then, Ohmic contacts were formed by depositing Ti/Al/Ni/Au (20/100/40/50 nm) followed by 775 °C rapid thermal anneal in N_2 atmosphere, yielding a contact resistance (R_c) of 0.35 Ω·mm. A 4 nm epitaxial $Mg_{0.25}Ca_{0.75}O$ dielectric capped with 2 nm of amorphous Al_2O_3 was then deposited by ALD. The growth temperature of MgCaO was 310 °C, using bis(*N*,*N’*-di-*tert*-butylacetamidinato)calcium, bis(*N*,*N’*-di-*sec*-butylacetamidinato) magnesium, and water vapor as precursors [5]. Single crystalline MgCaO offers an advantageous band offset, a good interface, and good lattice matching to GaN alloys [6]. Finally, Ni/Au (30/50 nm) was deposited as the gate metal followed by a lift-off process. All of the lithography processes were carried out using a MJB3 mask aligner lithography system. Devices have a gate width (W) of 100 μm and gate length (L_g) of 1, 2, 4, 8, 20, and 40 μm.

Fig. 3 shows the well-behaved DC output I_{ds}-V_{ds} characteristics of a GaN MOSHEMT. The device has an L_g=1 μm and source to drain spacing (L_{sd}) of 4.2 μm. Due to a 6 nm thick gate oxide, a high gate bias (V_{gs}) of 3 V can be applied, yielding a maximum drain current ($I_{ds,max}$) of 700 mA/mm. Fig. 4 is the I_{ds}-V_{gs} transfer characteristic measurement of the same device. Impressively, a high on/off ratio of 10^{10} is achieved with subthreshold swing (SS) of 65 mV/dec at V_{ds}=5 V. Traditional HEMT devices are not able to have such a high on/off ratio because of their large gate leakage currents in the off-state. The oxide of the MOSHEMT suppresses this leakage, yielding large on/off ratios. In addition, benefiting from the lattice matching and good interface between MgCaO and GaN,[5] the GaN MOSHEMT also demonstrates a negligible hysteresis (50 mV) as shown in Fig. 5. Fig. 6 shows the I_{ds}-V_{gs} and g_m-V_{gs} plot at the linear region. Peak transconductance ($g_{m,max}$) of 160 mS/mm and threshold voltage (V_T) of -2.2 V are observed at V_{ds}=5 V. The off-state breakdown/leakage characteristics of a MOSHEMT are shown in Fig.7. This device has a W/L_g=100 μm/1 μm and L_{gs}=L_{gd}=1.6 μm. The device is operated at the pinch-off region with V_{gs}=-3.5 V and V_s=0 V. It can be observed that the breakdown voltage is 150 V even with a short L_{gd}=1.6 μm. The breakdown voltage, which is a critical figure of merit for power switch, is expected to increase with the increase of L_{gd} and drain-gate region engineering. Scaling metrics of GaN MOSHEMTs are also studied as shown in Fig. 8 and Fig. 9. The I_{ds} and g_{max} are found to increase when the L_g is scaled. SS and drain induced barrier lowering (DIBL) are found to be slightly influenced by the L_g, and V_T shows roll-off behavior when L_g=1 μm.

In conclusion, we have demonstrated high performance AlGaN/GaN MOSHEMTs on Si substrate with high on/off ratio and high off-state breakdown voltage with epitaxial MgCaO gate dielectric. The lattice-matched MgCaO provides high quality interface and an appropriate electron barrier height, which makes it feasible to be applied to future GaN power switch applications.

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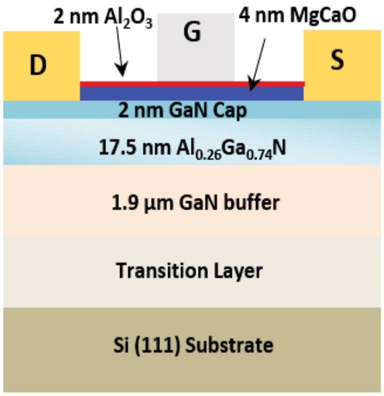

Fig. 1 Schematic view of an AlGaN/GaN MOSHEMT

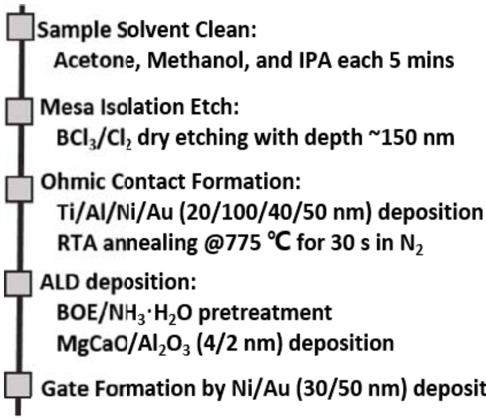

Fig. 2 Device fabrication process steps of AlGaN/GaN MOSHEMTs

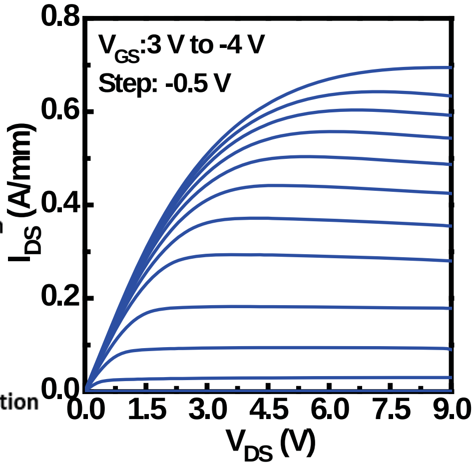

Fig. 3 Output characteristics of an AlGaN/GaN MOSHEMT with L_g=1 µm and L_{SD}=4.2 µm.

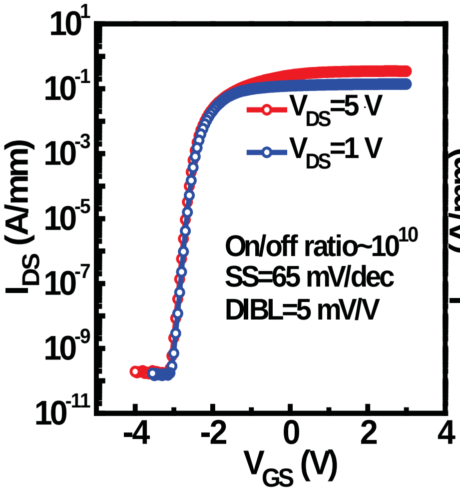

Fig. 4 I_{ds}-V_{gs} transfer characteristics with on/off ratio of 10^{10} and low SS=65 mV/dec.

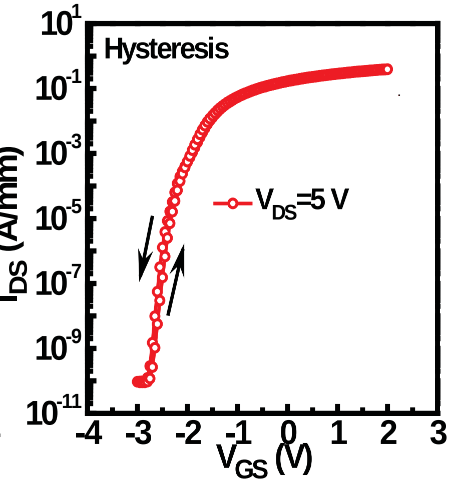

Fig. 5 I_{ds}-V_{gs} hysteresis measurement at V_{ds}=5 V.

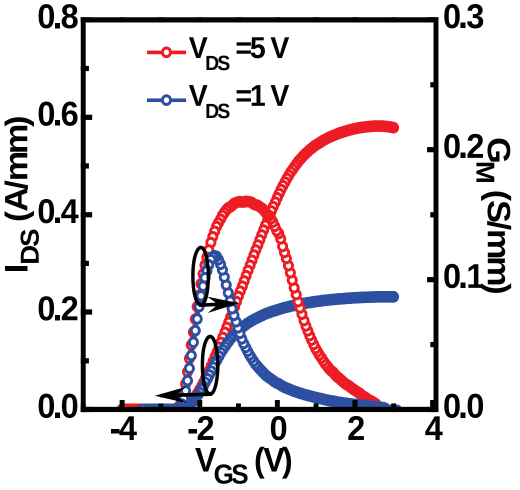

Fig. 6 I_{ds}-V_{gs} and g_m-V_{gs} of the same device in the linear region plot.

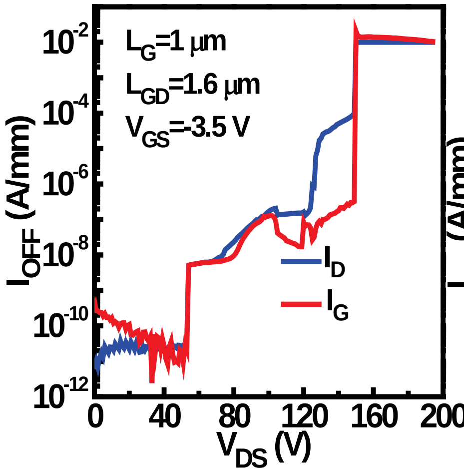

Fig. 7 Three-terminal off-state breakdown measurement with L_g=1 µm and L_{gd}=1.6 µm.

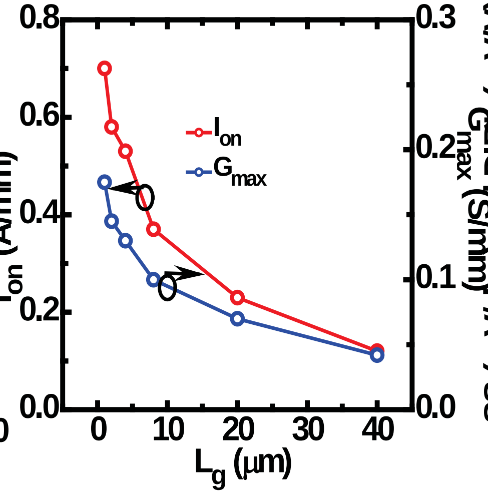

Fig. 8 I_{on} and G_{max} scaling metrics of GaN MOSHEMTs.

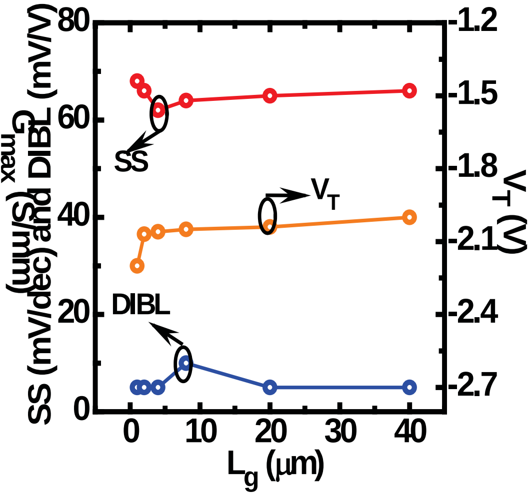

Fig. 9 SS, DIBL and V_T scaling metrics of GaN MOSHEMTs.