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Front and Back Contact Modification as a Route to Increasing Open Circuit Voltage in CZTS,Se Devices

Richard Haight
IBM T.J. Watson Research Center
PO Box 218 Yorktown Hts., NY 10598

FPACE II: Driving CZTS to the SQ Limit—Solving the Open Circuit Voltage Problem
The DoE Collaboration

- **IBM, Harvard, University of Delaware and UC San Diego**

  - **IBM**: Oki Gunawan, Talia Gershon, Yun S Lee (B8.09), Bruce Ek, Ravin Mankad, Tayfun Gokmen

  - **University of Delaware**: Brian McCandless, Doug Bishop (B6.13), Mike Lloyd

  - **Harvard**: Roy Gordon, Ashwin Jayaraman (B10.03), Mike Vogel, Danny Chua

  - **UC San Diego**: Andy Kummel, Kasra Sardashti (B5.04), Evgueny Chagarov (B5.10)
CdS/CZTS,Se Standard Device Architecture

- SODA LIME GLASS
- Mo layer back contact
- Transparent conducting oxide layer and AR coating
- CdS-chemical bath deposited-front contact
- CZTS,Se- spun on from solution or vapor deposited
- GBs
- Surface & Interface
- Metal wires to carry current
CdS/CZTS,Se Standard Device Architecture

Surface & Interface

GBs

Mo layer back contact

SODA LIME GLASS

CZTS,Se- spun on from solution
Or vapor deposited

Metal wires to carry current

Transparent conducting oxide layer and AR coating

CdS-chemical bath deposited-front contact
Surface & Interface

GBs

Transparent conducting oxide layer and AR coating

Metal wires to carry current

Cds-chemical bath deposited-front contact

Back contact issues

Mo layer back contact

SODA LIME GLASS
The Issues: 1-Bulk Defects

- CZTS,Se performance is dominated by 2 major issues:
  - Bulk defects (e.g. Cu-Zn antisites, Cu vacancies, point and cluster defects) - band tailing, band edge fluctuations ➞ impact Voc and hence Efficiency
  - DFT calculations show that Cu-Zn antisite and vacancy formation has very low energy barrier - (Chagarov B5.10)
The Issues: 2-Interfaces, Grain Boundaries, Contacts

The Challenges

1. Creating an oxide-free surface
2. Oxide-free surface is Cu depleted- is this good or bad for device performance?
3. What is the charge state of the bare surface?
4. Series of experiments (etching, Cu deposition) answers question 2
5. Grain boundaries- what’s there, how do we effectively passivate and what is the impact on device performance?
6. What about the back contact- can we replace MoS,Se?
7. How can we change the contacts in order to increase performance?
Attacking the Surface, Interface and Grain Boundary Problem

- Electron Spectroscopy: femtosecond-UPS and XPS
- SIMS to look at elemental distribution of CZTS, Se, Na and O vs. depth
- Photoluminescence Imaging
- Auger Nanoprobe- image grains and boundaries with ~8nm spatial resolution and chemical specificity (Sardashti, Kummel B5.04)
- Additionally
  - SEM, SFM
  - Kelvin Probe Force Microscopy (surface potentials)
Electronic Structure-UPS

CZTS,Se

vacuum level

Depletion region

Buffer (e.g. CdS)

Ionization Potential

IE_{abs}

E_{gap}

VB

CB

CdS

C-S/Laser System

UPS

26.35 eV

50 fs

CdS/CZTS,Se

 Binding Energy (eV)

Counts

IE_{abs}

E_f

14 12 10 8 6 4 2 0 -2

0 2000 4000 6000 8000 10000 12000
Electronic Structure-UPS + 1.55eV pump

Ionization Potential

$E_{\text{gap}}$

$E_{\text{abs}}$

CZTS,Se

Buffer

vacuum level

UPS

26.35 eV

1.55eV

50 fs

Co
cu

Ionization Potential

$E_F$

$E_{\text{F}}$

50 fs

UPS

CdS/CZTS,Se

Graph (binding energy vs. count)

© 2013 IBM Corporation
Electronic Structure-UPS +1.55eV Pump

CZTS,Se

Ionization Potential

vacuum level

CZTS,Se

Buffer

50 fs

26.35 eV

1.55eV

Flat Band For CZTS,Se

IE_{abs}

E_{gap}

CB

VB

UPS

IE_{Gap}

E_{F}

Counts

CdS/CZTS,Se

Binding Energy (eV)

© 2013 IBM Corporation
Heterojunction systems measured:
CdS, CdS+ In$_2$S$_3$, In$_2$S$_3$ CBD and ALD, ZnO, Zn(O,S), ZnS, Ga$_2$O$_3$, In$_2$O$_3$

APL 100, 193904 (2012)
APL 98, 253502 (2011)
MRS Bulletin dx.doi.org/10.1557/opl.2014.196
How Do We Produce an Oxide-Free CZTS,Se Surface?

- CZTS,Se is deposited via multiple layer solution phase or vapor deposited

- A “hard bake” (HB) is performed to crystallize and coarsen grains to 1-2µ average size ~600C

- Anneal in air (AA) (375C) is then carried out
  - (improves device performance)

- To create a good CdS interface (p-n jct) remove oxide
  - dilute NH₄OH treatment (also present in CdS bath)
Oxide-Free CZTS,Se Surface

In Accumulation

Haight, Shao, Wang, Mitzi
APL 104, 033902 (2014); doi: 10.1063/1.4862791

Neg charged
Cu vacancies
Post hard bake in $N_2$ glove box, we anneal the CZTS,Se in air to increase efficiency
Photoluminescence Imaging

**Hard Bake**

- HB

**Air Anneal**

- AA

PL spectroscopy using band pass filters

Peak of PL at ~0.96 eV

Band gap 1.13 eV

**Energy (eV)**

- 0.78
- 0.83
- 0.89
- 0.96
- 1.04
- 1.13
- 1.24

**Wavelength (nm)**

- 800
- 900
- 1000
- 1100
- 1200
- 1300
- 1400
- 1500
- 1600
- 1700

**Relative PL Intensity**

- 10
- 100
- 1000
- 10000

**Figure 1.** Photoluminescence imaging of as-deposited films with different treatments. **PL** spectroscopy using band pass filters reveals the peak of PL at ~0.96 eV, and the band gap is 1.13 eV. (From APL 104, 033902 (2014))
O diffusing Into bulk

Depth (microns)

Concentration (10^19 a/cc)

SIMS

APL 104, 033902 (2014)
Auger Nanoprobe (Sardashti B5.04 yesterday)

Hard Bake + 5 min NH$_4$OH etch- no air exposure

Hard Bake + Air Anneal + 5 min NH$_4$OH etch

Sardashti et. al. Adv. En. Mat. 2015, 1402180
Key Surface and Grain Boundary Results

- Surface is Cu depleted
- $\text{SnO}_x$ forms at surface and dresses grain boundaries $\Rightarrow$ passivation
- Selenates form at surface and grain boundaries
- Na present in oxide, removed with NH$_4$OH, present along grain boundaries
- Air anneal drives O into film along grain boundaries-forms SnO$_x$ throughout the film
Is a Cu Depleted Surface Good?  
Add Cu to Surface to Find Out

- Deposit Cu → changes BB from accumulation to depletion
  eradicates neg surface charge

- \( \text{H}_2\text{O}_2 + \text{NH}_4\text{OH} \) (Kummel, Sardashti UC San Diego)
  - \( \text{H}_2\text{O}_2 \) oxidizes and \( \text{NH}_4\text{OH} \) reduces the oxide
    thereby etching into the surface- produces a surface with higher Cu content
Increase Cu Content in Surface - What Happens to Device Performance?

- **Cu depleted surface extremely important**

- **$H_2O_2$ also removes passivating oxide near surface** leads to significant recombination at buffer/absorber bndry
What we have learned about the surface and grain boundaries

- Surface is **Cu depleted** and exhibits upward band bending
  - result of negative charge at/near surface ➔ ionized Cu vacancies

- Air anneal results in GB passivation
  - greater PL intensity and higher device performance
  - SIMS shows O throughout film- fast diffusion along GB ➔ SnO$_x$ formation passivates GB
  - **Auger nanoprobe: SnO$_x$ observed at GBs, this passivates GBs**

- Cu depleted surface + passivation up to buffer/absorber interface critical for optimal device performance

- **Model for P-N Jct:** Chemical bath deposition of CdS, Cd$^{2+}$ occupies Cu vacancies, dopes n-type—very similar to CIGS (NREL, Rockett)
New Buffer Materials

Ga$_2$O$_3$/CZTS,Se

Counts

Binding Energy (eV)

CZTS,Se  Ga$_2$O$_3$

In$_2$S$_3$ and In$_2$ (O$_x$S$_{3-x}$) Jayaraman, B10.03 tomorrow
How Can We Increase $V_{oc}$ and Efficiency?

Two Possible Approaches

- We can solve the bulk defect problem
  - Ongoing work at IBM, UDel, UCSD

- We can modify back contact
  - High WF combined with thin absorber
  - The physics behind this:
How Can We Increase $V_{oc}$ and Efficiency?
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Backwall Superstrate: Larsen, Simchi, Xin, Kim, Shafarman, APL 104, 033901, 2014
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Two Possible Approaches

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- We can modify back contact
  - High WF combined with thin absorber
  - The physics behind this:

\[
\begin{align*}
\text{MoO}_3 / \text{CZTS,Se} \\
\text{MoO}_3 & \quad \text{CZTS,Se} \\
\end{align*}
\]

\[
\begin{align*}
\text{WF} &= 6.5 \text{ eV} \\
\text{BB} &= -180 \text{ meV}
\end{align*}
\]
Hall Measurements

Carrier Density, \( \text{MoO}_3 \)

\[ \mu = 0.1 \, \text{cm}^2/\text{Vs} \]
(Meas. at 350 C, assumed to be fixed throughout)

WF remains >6 eV
For all temps

Gunawan and Haight
High Work Function Back Contacts

Tayfun Gokmen
WXAMPS study
AEM 2015, 1402180
Summary

- Increased understanding of surface and grain boundaries
- **For good efficiencies:**
  - Cu depleted surface a requirement, oxide-free surface has lots of Cu vacancies (neg. charged)
  - passivated grain boundaries- our approach forms SnOx along GBs, inhibits e-h recombination
  - Cd diffuses into Cu vacancies at surface- similar to CIGSe-forming high quality p-n junction
  - To improve efficiency
    - address bulk defects- antisites, vacancies
    - back contact modification + film thickness optimization to achieve higher Voc
Backup Slides
Tin Oxide

Sn 4d

Counts

Binding Energy (eV)

APL 104, 033902 (2014)