Advanced atomic layer deposition and epitaxy processes

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Advanced Atomic Layer Deposition and Epitaxy Processes

Roy Gordon
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Harvard University
Single-crystal oxide insulators grown epitaxially on GaAs, Ge and GaN by ALE

Outline

Atomic Layer Epitaxy (ALE)

ALE of single-crystal La$_2$O$_3$ on GaAs(111)

CMOS circuits with La$_2$O$_3$ on GaAs(111)

ALE of single-crystal La$_2$O$_3$ on Ge(111)

ALE of single-crystal (Mg,Ca)O on GaN(0001)
ITRS roadmap

High $\mu$ + high $k$
**GaAs has Many Traps at Oxide Interfaces**

- Very large frequency dispersion
- Very low drive currents

- ~$10^{13}$ cm$^{-2}$ traps at GaAs interface with oxides
- $<10^{11}$ cm$^{-2}$ traps at Si/SiO$_2$ interface
- GaAs MOS transistors are much poorer than Si

Solution: epitaxial single-crystal La$_2$O$_3$ on GaAs

- ~$10^{11}$ cm$^{-2}$ traps at GaAs/La$_2$O$_3$ interface
- First CMOS transistors ever made on GaAs
**Atomic Layer Epitaxy (ALE)**

Sequential, self-limiting surface reactions make alternating layers:

Benefits of ALE:

- High-quality epitaxial interfaces with few traps
- Atomic level of control over film composition
  \[ \Rightarrow \text{nanolaminates and multi-component materials} \]
- Uniform thickness over large areas and inside narrow holes
- Smooth surfaces
- High density and few defects or pinholes
- Low deposition temperatures (for very reactive precursors)
- Pure films (for suitably reactive precursors)
- Full-wafer semiconductor-grade production equipment available
Amidinate Precursors for Trivalent Metals

La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Y, Sc, In, Ru, Ti

R = H (formamidinate, fmd)
R = CH₃ (acetamidinate, amd)

Now produced commercially by the Dow Chemical Company
Vaporization of Lanthanum Amidinate Precursor

tris(N,N′-diisopropyl-formamidinato)lanthanum
La((iPr₂N)₂CH)₃
abbreviated La(fmd)₃

Most volatile lanthanum compound known

Complete evaporation without decomposition or residue
ALE of Lanthanum Oxide, $\text{La}_2\text{O}_3$

Precursors: $\text{H}_2\text{O}$ and $\text{La(fmd)}_3$

$\text{La(fmd)}_3$ at 120 °C, substrate at 300 °C

slope => 0.16 nm per cycle

line starts at origin => no delay in nucleation
ALE $\text{La}_2\text{O}_3$ is Epitaxial on GaAs(111)A

Lattice Constant Matching:

$$a(\text{La}_2\text{O}_3) = 2.0008 \times a(\text{GaAs})$$

or 0.04% mismatch
Atomic layer epitaxy of GaAs(111)/La₂O₃

Side view of GaAs(111)A/La₂O₃

Top view
CV characteristics of GaAs(111)/La$_{2-x}$Y$_x$O$_3$

Closer Lattice Match to GaAs => less dispersion

Mismatch => -3.32 % -0.64 % +0.04 %
Interface Trap Densities

\[ D_{it} \text{ (cm}^{-2}\text{eV}^{-1}) \]

- \( \text{Al}_2\text{O}_3/\text{GaAs}(111)\text{A} \)
- \( \text{La}_{1.1}\text{Y}_{0.9}\text{O}_3/\text{GaAs}(111)\text{A} \) -3.3%
- \( \text{La}_2\text{O}_3/\text{GaAs}(111)\text{A} \) +0.04%

Temperature:
- 150°C
- 90°C
- 25°C
Closer Lattice Match to GaAs => Fewer Traps

- $2 \times 10^{11}$ traps cm$^{-2}$
- $\text{La}_2\text{O}_3$
- $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$
- $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$
- $\text{a-Al}_2\text{O}_3$

trap density (in units of $10^{12}$ cm$^{-2}$)

lattice mismatch (%)

1 x 10^4 to 1 x 10^6
Summary of GaAs CMOS

- **pMOSFET**
- **nMOSFET**

- **Ni/Au**
- **PtTi**
- **GeNiAu**
- **Ti/Au**

- **Common substrate**
- **Common dielectric**
- **ALE integration**
- **High quality interface**
GaAs nMOSFET with La$_2$O$_3$ epitaxial dielectrics

- High drain current of 376 mA/mm is obtained from GaAs nMOSFET with 1μm gate length
- Current $I_{on}/I_{off} \sim 10^7$, subthreshold slope as low as 74 mV/dec
- A mean $D_{it}$ of $1.7 \times 10^{12}$ cm$^{-2}$·eV$^{-1}$, using $SS = 60(1+qD_{it}/C_{ox})$
GaAs nMOSFET with La$_2$O$_3$ epitaxial dielectric

- Peak transconductance $G_m \sim 190$ mS/mm
- Peak electron effective mobility $\sim 1150$ cm$^2$/Vs
GaAs pMOSFET with La$_2$O$_3$ epitaxial dielectric

- Maximum drain current of 30 mA/mm is obtained from GaAs pMOSFET with 1µm gate length
- $I_{on}/I_{off} \sim 10^4$ and $\sim 10^3$ for the pMOSFETs with 1µm gate length annealed at 780°C and 800°C, respectively
A transconductance of \( 12 \text{ mS/mm} \) is obtained from GaAs pMOSFET with \( L_g = 1 \mu\text{m} \).

The peak effective hole mobility is around \( 180 \text{ cm}^2/\text{Vs} \).
CMOS GaAs inverters

- Peak gain of 12 is obtained with $V_{DD} = 3V$
CMOS GaAs NAND logic gate

**Input Values:**
- $V_{in,a}$: 1 0 1 0
- $V_{in,b}$: 1 1 0 0

**Output Value:**
- $V_{out}$: 0 1 1 1

**Truth Table:**

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<th>$V_{in,a}$</th>
<th>$V_{in,b}$</th>
<th>$V_{out}$</th>
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<tr>
<td>A</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>1</td>
<td>1</td>
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CMOS GaAs NOR logic gate

(a) CMOS GaAs NOR gate

(b) NOR gate circuit diagram

V\text{in,a} = 1, \quad V\text{in,b} = 0, \quad V\text{out} = 1

V\text{in,a} = 0, \quad V\text{in,b} = 1, \quad V\text{out} = 0

V\text{in,a} = 1, \quad V\text{in,b} = 1, \quad V\text{out} = 0

V\text{in,a} = 0, \quad V\text{in,b} = 0, \quad V\text{out} = 1
CMOS GaAs 5-stage ring oscillator

5 inverters connected in series mode

\[ V_{o} \]

\[ V_{DD} \]

\[ V_{SS} \]
CMOS GaAs 5-stage ring oscillator

At \( V_{DD} = 2 \text{ V} \), the fundamental oscillation frequency is at 2.2 MHz.

The fundamental resonance frequency increases from 0.35 MHz at \( V_{DD} = 1 \text{ V} \) to 3.87 MHz at \( V_{DD} = 2.75 \text{ V} \).

Acknowledgement: Y.Q. Wu/HUST
How to Translate these Results to GaAs(100)

ALE La$_2$O$_3$ and LaLuO$_3$ are polycrystalline, not epitaxial, on GaAs(100)

Electrical measurements of capacitors show many traps at interface
Wet Etching GaAs(100) Exposes (111) Surface

Rightarrow epitaxial La$_2$O$_3$ on GaAs(111) facets
Orientation to Form GaAs(111) Facets

GaAs(100) Substrate
(011)

Wave Patterned Direction
(01\bar{1})

Gate

Pattern along (01\bar{1})
WaveFET Structure on GaAs(100)

(a)

Source
La$_2$O$_3$ + Al$_2$O$_3$

Ti/Au Gate

Wave Channel
GaAs(100) substrate

(b)

A—A'

WaveFET Structure on GaAs(100)

Ti/Au Gate
10nm Al$_2$O$_3$
5nm La$_2$O$_3$
GaAs(100) substrate
WaveFET GaAs Transistor Performance

(a) $V_{GS}$ from 0V to 4V in 0.5V step

(b) $L_g = 1\mu m$

(c) $g_{m,max} (2V) = 32\text{mS/mm}$

(d) $R_{sd} = 1.62\Omega \cdot \text{mm}$

- $SS (V_{ds} = 0.05V) = 135\text{mV/dec}$
- $SS (V_{ds} = 2\text{V}) = 184\text{mV/dec}$
- $DIBL = 65\text{mV/V}$

$V_{DS} = 0.05\text{V}$

$V_{ID} (\text{mA/mm})$

$V_{GS} (\text{V})$

$V_{DS} = 2\text{V}$

$g_m (\text{mS/mm})$

$V_{DS} = 2\text{V}$

$g_m, \text{max} (2\text{V}) = 32\text{mS/mm}$

$V_{DS} = 0.05\text{V}$

$g_m (\text{mS/mm})$

$V_{GS} (\text{V})$

$R_{tot} (\text{k}\Omega)$

$L_g (\mu m)$

$\Delta L = 0.36\mu m$
Epitaxy of $\text{La}_{1.7}\text{Y}_{0.3}\text{O}_3$ on Ge(111)
Capacitors with (La,Y)$_2$O$_3$ on Ge(111)

High-performance pMOS transistors are expected using this epitaxial interface.
Possible Epitaxial Oxides for GaN

Ge, GaAs & AlAs (1.13) match $\text{La}_2\text{O}_3$
Si, GaP & AlP (1.09) match $\text{La}_{0.6}\text{Y}_{1.4}\text{O}_3$

GaN (0.90) $\text{Mg}_x\text{Ca}_{1-x}\text{O}$

Ca => CaO too large for perfect epitaxy on GaN
Mg => MgO too small for perfect epitaxy on GaN
Phase Diagram of \((\text{Ca,Mg})\text{O}\)

Miscibility gap for most compositions

Metastable compositions decompose at about 600 °C

=> Need to deposit \((\text{Ca,Mg})\text{O}\) at \(T < 600 \, ^\circ\text{C}\) to avoid decomposition

Phase equilibrium diagram for the system \(\text{CaO–MgO}\). Solid

J. Am. Ceram. Soc. 46, 314 (1963)
2 Precursors for ALE of Magnesium Oxide, MgO

\[
\text{bis}(N,N'\text{-di-sec-butylacetamidinato}) \quad \text{magnesium}
\]

\[
\text{bis}(N,N'\text{-di-tert-butylacetamidinato}) \quad \text{magnesium}
\]

\[
\text{Liquid}
\]

\[
\text{Solid}
\]

ALD bubbler temperatures 90 – 110 °C

Residue < 1% (clean evaporation)

Chose the liquid on left because of its ready purification by distillation and easier handling

ALD of MgO at 300 °C, low enough to avoid thermal decomposition of (Ca,Mg)O
3 Precursors for ALE of Calcium Oxide

**Superior precursor:**
- Highest volatility
- Reactive to H₂O
- Scaled up production

**bis(N,N’-di-tert-butyl-acetamidinato) calcium**
- Sublimes at 185-190°C
- Low volatility
- Reactive to H₂O

**bis(N,N’-diisopropyl-acetamidinato) calcium**
- Sublimes at 135-140°C
- Higher volatility
- Reactive to H₂O

**bis(N,N’-diisopropyl-formamidinato) calcium**
- Sublimes at 95-100°C
- Superior precursor:
  - Highest volatility
  - Reactive to H₂O
  - Scaled up production

**Notes:**
ALD of CaO at 300 °C, low enough to avoid decomposition of (Ca,Mg)O
Electron Diffraction from Epitaxial (Ca,Mg)O on GaN(0001)

Epitaxial orientation:
(Ca,Mg)O(111) // GaN (0001)

Beam Direction [11-20]
Composition of (Ca,Mg)O by RBS on Carbon Substrates

Aluminum in capping layer of ALD Al₂O₃
Lattice Constant Mismatch

Dosing ratio Mg:Ca=1:3; RBS: Mg:Ca=1:3

2theta=71.09 \( d = 1.325 \text{nm} \) mismatch = 2.2% 
(Vegard’s law prediction: mismatch = 3.7%)

2theta Omega scan
MgCaO 222 too much Ca for perfect lattice match

Rocking scan
FWHM=0.23deg
(Ca,Mg)O is a good insulator on GaN or InAlN

Large band offsets for both conduction and valence bands of MgO

Materials 2012, 5, 1297-1335
Capacitor with (Mg,Ca)O on InAlN => Very Few Traps

Almost no frequency dispersion => few states at the interface.

AC conductance extracts very low $D_{it}$ in the bandgap, around $10^{11} \text{ cm}^{-2}$
The (Mg,Ca)O gate insulator reduced the gate leakage by four orders of magnitude, from $10^{-8}$ to $10^{-12}$ A/mm.

The subthreshold slope is nearly ideal at 64 mV/dec.
Summary

Atomic Layer Epitaxy (ALE) forms high-quality epitaxial interfaces

ALE $\text{La}_2\text{O}_3/\text{GaAs}(111)$ => both p- and n- type capacitors with low dispersion

=> the first CMOS circuits with both channels in GaAs

ALE $\text{La}_2\text{O}_3/\text{Ge}(111)$ => epitaxial structures

ALE (Mg,Ca)O/GaN or InAlN => capacitors with low dispersion

ALE (Mg,Ca)O/InAlN => transistors with low gate leakage

ALE is a scalable process for making high-performance devices
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