Advanced atomic layer deposition and epitaxy processes

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Advanced Atomic Layer Deposition and Epitaxy Processes

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Single-crystal oxide insulators grown epitaxially on GaAs, Ge and GaN by ALE

Outline

Atomic Layer Epitaxy (ALE)

ALE of single-crystal La$_2$O$_3$ on GaAs(111)

CMOS circuits with La$_2$O$_3$ on GaAs(111)

ALE of single-crystal La$_2$O$_3$ on Ge(111)

ALE of single-crystal (Mg,Ca)O on GaN(0001)
ITRS roadmap

High $\mu$ + high $k$
GaAs has Many Traps at Oxide Interfaces

=> very large frequency dispersion

~$10^{13}$ cm$^{-2}$ traps at GaAs interface with oxides

< $10^{11}$ cm$^{-2}$ traps at Si/SiO$_2$ interface

=> GaAs MOS transistors are much poorer than Si

Solution: epitaxial single-crystal La$_2$O$_3$ on GaAs

⇒ ~$10^{11}$ cm$^{-2}$ traps at GaAs/La$_2$O$_3$ interface

⇒ First CMOS transistors ever made on GaAs
Atomic Layer Epitaxy (ALE)

Sequential, self-limiting surface reactions make alternating layers:

Benefits of ALE:

- High-quality epitaxial interfaces with few traps
- Atomic level of control over film composition
  ⇒ nanolaminates and multi-component materials
- Uniform thickness over large areas and inside narrow holes
- Smooth surfaces
- High density and few defects or pinholes
- Low deposition temperatures (for very reactive precursors)
- Pure films (for suitably reactive precursors)
- Full-wafer semiconductor-grade production equipment available
Amidinate Precursors for Trivalent Metals

La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Y, Sc, In, Ru, Ti

R = H (formamidinate, fmd)
R = CH₃ (acetamidinate, amd)

Now produced commercially by the Dow Chemical Company
Vaporization of Lanthanum Amidinate Precursor

tрис(Н,Н’-диизопропил-формамидинато)ланthanум
La((iPr₂N)₂CH)₃
abbreviated La(fmd)₃

Most volatile lanthanum compound known

Complete evaporation without decomposition or residue
ALE of Lanthanum Oxide, La$_2$O$_3$

Precursors: H$_2$O and La(fmd)$_3$

La(fmd)$_3$ at 120 °C, substrate at 300 °C

slope => 0.16 nm per cycle

line starts at origin => no delay in nucleation
ALE $\text{La}_2\text{O}_3$ is Epitaxial on GaAs(111)A

TEM

High Resolution XRD

Lattice Constant Matching:

$a(\text{La}_2\text{O}_3) = 2.0008 \times a(\text{GaAs})$

or 0.04% mismatch
Atomic layer epitaxy of GaAs(111)/La$_2$O$_3$

Side view of GaAs(111)A/La$_2$O$_3$

top view
CV characteristics of GaAs(111)/La$_{2-x}$Y$_x$O$_3$

Closer Lattice Match to GaAs $\Rightarrow$ less dispersion

Mismatch $\Rightarrow$ -3.32 %, -0.64 %, +0.04 %
Interface Trap Densities

\[ D_{it} \text{ (cm}^{-2}\text{eV}^{-1}) \]

- \( \text{Al}_2\text{O}_3/\text{GaAs}(111)A \)
- \( \text{La}_{1.1}\text{Y}_{0.9}\text{O}_3/\text{GaAs}(111)A \) -3.3%
- \( \text{La}_2\text{O}_3/\text{GaAs}(111)A \) +0.04%

\( T = 150^\circ C \)
\( T = 90^\circ C \)
\( T = 25^\circ C \)
Closer Lattice Match to GaAs $\Rightarrow$ Fewer Traps

![Graph showing the correlation between trap density and lattice mismatch, with specific compounds and trap densities labeled.]
Summary of GaAs CMOS
GaAs nMOSFET with La$_2$O$_3$ epitaxial dielectrics

- High drain current of 376 mA/mm is obtained from GaAs nMOSFET with 1μm gate length
- Current $I_{on}/I_{off} \sim 10^7$, subthreshold slope as low as 74 mV/dec
- A mean $D_{it}$ of $1.7\times10^{12}$ cm$^{-2}$·eV$^{-1}$, using $SS = 60(1+qD_{it}/C_{ox})$
GaAs nMOSFET with La$_2$O$_3$ epitaxial dielectric

- Peak transconductance $G_m \approx 190$ mS/mm
- Peak electron effective mobility $\mu_{n,\text{peak}} \approx 1150$ cm$^2$/Vs
GaAs pMOSFET with La$_2$O$_3$ epitaxial dielectric

- Maximum drain current of 30 mA/mm is obtained from GaAs pMOSFET with 1μm gate length
- $I_{on}/I_{off} \sim 10^4$ and $\sim 10^3$ for the pMOSFETs with 1μm gate length annealed at 780°C and 800°C, respectively
GaAs pMOSFET with La$_2$O$_3$ epitaxial dielectric

- A transconductance of $12 \text{ mS/mm}$ is obtained from GaAs pMOSFET with $L_g = 1\mu m$.
- The peak effective hole mobility is around $180 \text{ cm}^2/\text{Vs}$.
CMOS GaAs inverters

- Peak gain of 12 is obtained with $V_{DD} = 3V$
CMOS GaAs NAND logic gate

(a) CMOS GaAs NAND logic gate image.

(b) Circuit diagram of a CMOS GaAs NAND logic gate.

Inputs:
- $V_{\text{in},a}$: 1 0 1 0
- $V_{\text{in},b}$: 1 1 0 0

Output:
- $V_{\text{out}}$: 0 1 1 1

Waveform diagrams showing input and output signals over time.
CMOS GaAs NOR logic gate

- Inputs:
  - \( V_{\text{in},a} \): 1 0 1 1
  - \( V_{\text{in},b} \): 1 1 0 0

- Output:
  - \( V_{\text{out}} \): 0 0 0 1

- NOR gate diagram:
  - Diagram labeled (a) shows the physical implementation of the NOR gate.
  - Diagram labeled (b) shows the equivalent circuit diagram.

- Time response:
  - Waveform showing the NOR gate response with inputs and outputs.
  - Timing graph illustrating the logic levels over time.
CMOS GaAs 5-stage ring oscillator

5 inverters connected in series mode

VDD

VSS

Vo

VDD

VSS

Vo

Ring Osc. 2um
CMOS GaAs 5-stage ring oscillator

- At $V_{DD} = 2$ V, the fundamental oscillation frequency is at 2.2 MHz.
- The fundamental resonance frequency increases from 0.35 MHz at $V_{DD} = 1$ V to 3.87 MHz at $V_{DD} = 2.75$ V.

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How to Translate these Results to GaAs(100)

ALE La$_2$O$_3$ and LaLuO$_3$ are polycrystalline, not epitaxial, on GaAs(100)

Electrical measurements of capacitors show many traps at interface
Wet Etching GaAs(100) Exposes (111) Surface

=> epitaxial La$_2$O$_3$ on GaAs(111) facets
Orientation to Form GaAs(111) Facets

GaAs(100) Substrate

Wave Patterned Direction

Pattern along (011)
WaveFET Structure on GaAs(100)

Device schematic:
- Ti/Au Gate
- 10nm Al₂O₃
- 5nm La₂O₃
- GaAs(100) substrate
WaveFET GaAs Transistor Performance

(a) Voltage transfer characteristic

- $V_{GS}$ from 0V to 4V in 0.5V step
- $I_D$ (mA/mm) vs $V_{DS}$ (V)

(b) Output characteristic

- $L_g = 1\mu m$
- $V_{DS} = 2V$
- $V_{DS} = 0.05V$
- $I_D$ (mA/mm) vs $V_{GS}$ (V)

(c) Transconductance

- $g_{m,\text{max}} (2V) = 32\text{mS/mm}$
- $V_{DS} = 2V$
- $V_{DS} = 0.05V$
- $g_m$ (mS/mm) vs $V_{GS}$ (V)

(d) Total resistance

- $I_{on}$ ($V_{GS} - V_T = 1V$)
- $I_{on}$ ($V_{GS} - V_T = 1.5V$)
- $I_{on}$ ($V_{GS} - V_T = 2V$)
- $I_{on}$ ($V_{GS} - V_T = 2.5V$)
- $R_{tot}$ (kΩ) vs $L_g$ (µm)

- $R_{sd} = 1.62\Omega\cdot\text{mm}$
- $\Delta L = 0.36\mu m$
Epitaxy of $\text{La}_{1.7}\text{Y}_{0.3}\text{O}_3$ on Ge(111)
Capacitors with (La,Y)$_2$O$_3$ on Ge(111)

High-performance pMOS transistors are expected using this epitaxial interface
Possible Epitaxial Oxides for GaN

- Ge, GaAs & AlAs (1.13) match La$_2$O$_3$
- Si, GaP & AlP (1.09) match La$_{0.6}$Y$_{1.4}$O$_3$
- GaN (0.90)
- Mg$_x$Ca$_{1-x}$O

- Mg => MgO too small for perfect epitaxy on GaN
- Ca => CaO too large for perfect epitaxy on GaN

Ionic radius (pm)
Cubic lattice constant (nm)
Phase Diagram of \((\text{Ca},\text{Mg})\text{O}\)

Miscibility gap for most compositions

Metastable compositions decompose at about 600 °C

=> Need to deposit \((\text{Ca},\text{Mg})\text{O}\) at \(T < 600 \, ^\circ\text{C}\) to avoid decomposition

Phase equilibrium diagram for the system \(\text{CaO}–\text{MgO}\). Solid

2 Precursors for ALE of Magnesium Oxide, MgO

**bis(\(N,N'\)-di-sec-butylacetamidinato) magnesium**

**bis(\(N,N'\)-di-tert-butylacetamidinato) magnesium**

ALD bubbler temperatures 90 – 110 °C

Residue < 1% (clean evaporation)

Chose the liquid on left because of its ready purification by distillation and easier handling

ALD of MgO at 300 °C, low enough to avoid thermal decomposition of (Ca,Mg)O
3 Precursors for ALE of Calcium Oxide

\[
\text{bis}(N,N'\text{-di-}\text{tert-}\text{butyl-}\text{acetamidinato}) \quad \text{calcium}
\]

Sublimes at 185-190°C
Low volatility
Reactive to H\text{2}O

\[
\text{bis}(N,N'\text{-diisopropyl-}\text{acetamidinato}) \quad \text{calcium}
\]

Sublimes at 135-140°C
Higher volatility
Reactive to H\text{2}O

\[
\text{bis}(N,N'\text{-diisopropyl-}\text{formamidinato}) \quad \text{calcium}
\]

Sublimes at 95-100°C
Superior precursor:
Highest volatility
Reactive to H\text{2}O
Scaled up production

ALD of CaO at 300 °C, low enough to avoid decomposition of (Ca,Mg)O
Electron Diffraction from Epitaxial (Ca,Mg)O on GaN(0001)

Epitaxial orientation:
(Ca,Mg)O(111) // GaN (0001)

Beam Direction [11-20]
Composition of \((\text{Ca,Mg})\text{O}\) by RBS on Carbon Substrates

Aluminum in capping layer of ALD \(\text{Al}_2\text{O}_3\)
Lattice Constant Mismatch

Dosing ratio Mg:Ca=1:3; RBS: Mg:Ca=1:3

2theta=71.09 d=1.325nm  mismatch = 2.2%
(Vegard’s law prediction: mismatch = 3.7%)

too much Ca for perfect lattice match

2theta Omega scan

GaN 0004
MgCaO 222

Rocking scan

FWHM=0.23deg
(Ca,Mg)O is a good insulator on GaN or InAlN

Large band offsets for both conduction and valence bands of MgO

Materials 2012, 5, 1297-1335
Capacitor with (Mg,Ca)O on InAlN => Very Few Traps

Almost no frequency dispersion => few states at the interface.

AC conductance extracts very low $D_{it}$ in the bandgap, around $10^{11}$ cm$^{-2}$.
The (Mg,Ca)O gate insulator reduced the gate leakage by four orders of magnitude, from $10^{-8}$ to $10^{-12}$ A/mm.

The subthreshold slope is nearly ideal at 64 mV/dec.
Atomic Layer Epitaxy (ALE) forms high-quality epitaxial interfaces

ALE La$_2$O$_3$/GaAs(111) => both p- and n- type capacitors with low dispersion

=> the first CMOS circuits with both channels in GaAs

ALE La$_2$O$_3$/Ge(111) => epitaxial structures

ALE (Mg,Ca)O/GaN or InAlN => capacitors with low dispersion

ALE (Mg,Ca)O/InAlN => transistors with low gate leakage

ALE is a scalable process for making high-performance devices
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