Quantitative Evaluation of Cobalt Disilicide/Si Interfacial Roughness

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Abstract

The formation of smooth, conformal cobalt disilicide ($CoSi_2$) without facets or voids is critical for microelectronic device reliability owing to the ultra-shallow contact areas. Here we demonstrate the formation of smooth and conformal $CoSi_2$ films by chemical vapor deposition (CVD) of cobalt nitride (Co_xN) films on silicon (Si) or on silicon on insulator (SOI) substrates, followed by in-situ rapid thermal annealing (RTA) at 700°C. To reveal the $CoSi_2$/Si interfacial morphology, we report a back-to-front sample preparation method, in which mechanical polishing, anisotropic tetramethylammonium hydroxide (TMAH) wet etching, hydrofluoric acid (HF) wet etching, and isotropic xenon difluoride (XeF_2) dry etching are employed to remove the SOI substrate from the back side to expose the $CoSi_2$/Si interface. This method offers a robust and reliable procedure for quantitative assessment of the $CoSi_2$/Si interfacial roughness, as well as analytical support for advanced fabrication process development.

Introduction

Metal silicides have been widely used as self-aligned contacts in silicon-based microelectronic devices for the past decades.[1] Among various metal silicides, $CoSi_2$ is considered as an attractive contact material because of its low resistivity (10-20 μΩ·cm), no line-width dependence in narrow lines, and its superior chemical and thermal stability.[2-4] $CoSi_2$ has been used for various electronic devices, such as memory electrode for 3D structure[5] and the metallization material for nanoparticles, nanowires[6, 7]. As devices scale down, a thin, uniform $CoSi_2$ layer is essential for those nano-electronic applications. Otherwise, cobalt silicide spikes will cause severe junction leakage and lead to device failure.[8] However, the complicated growth mechanism of $CoSi_2$ can result in a problematic, rough $CoSi_2$/Si interface.[9] [10] The complex kinetics results from several concurrent mechanisms: nucleation, diffusion and perhaps interface reaction.[11] Many efforts have been focused on the formation of a smooth $CoSi_2$ interface with Si by optimizing the fabrication process. For example, a Ti capping layer was introduced to reduce interfacial roughness induced by ambient contamination.[12] Hence, the quantitative evaluation of the $CoSi_2$/Si interfacial roughness is crucial for optimization of fabrication processes for $CoSi_2$.

$CoSi_2$ is typically fabricated by annealing sputtered Co films on active source, drain and gate regions.[2] However, the conventional sputtering process results in poor step coverage and induces high ion damage in the active regions, making it undesirable for complex 3D architectures in modern transistors. Chemical vapor deposition (CVD) can avoid these problems by producing conformal cobalt-containing thin films without ion-induced damage.[13-15]

In this paper, we evaluate quantitatively the roughness of the cobalt silicide/Si interface, in which the cobalt silicide is produced from CVD-deposited Co_xN by in-situ RTA at 700°C. The CVD process produced smooth, uniform and highly conformal Co_xN, and also resulted in a smooth and high-quality $CoSi_2$/Si interface.[13] To reveal the $CoSi_2$/Si interface for analysis of its roughness, we adapted and modified a SIMS sample preparation technique to remove the backside of the sample. This method uses both wet-etching and dry etching to remove a SOI substrate below the $CoSi_2$. This work provides direct quantitative assessment of cobalt silicide/Si interfacial roughness for the first time, and offers critical insights for future process optimization.

Experimental

Cobalt nitride films on Si and SOI substrates were prepared by CVD using bis(*N-tert*-butyl-*N'*-ethyl-propionamidinato) cobalt(II) and a mixture of 20 sccm NH_3 and 40 sccm H_2 at 200°C. The details of this process have been described elsewhere.[13] The Si and SOI substrates were first treated by UV-ozone and then cleaned by HF before deposition. After cleaning, the substrates were immediately placed into the reactor chamber and evacuated, to suppress oxidation of the substrates. As Co is unable to react with SiO_2,[12] the cobalt silicide formation might be slowed down or even blocked by any interfacial native oxide. Therefore, a clean substrate without native oxide is critical to obtain a uniform and smooth $CoSi_2$ films.

The as-deposited Co_xN films were treated by *in-situ* RTA at elevated temperatures from 500°C to 700°C for 30 sec in purified N_2. Those gases used in the deposition and annealing

processes were purified by gas purifiers (Entegris Gatekeeper) to reduce the impurities below 1 ppb for all contaminants including O_2, CO, CO_2, and H_2O. This purification is needed because the $CoSi_2$ formation process is highly sensitive to traces of oxygen-containing impurities in the annealing ambient.[16] Extremely low levels of these impurities are essential for smooth $CoSi_2$ formation.[12] Indeed, attempts to form $CoSi_2$ from Co_xN by ex-situ RTA were unsuccessful owing to the sample contamination during the exposure to the air and the annealing ambient (our *ex-situ* RTA tool does not use purified gas for annealing). Those impurities resulted in discontinuous $CoSi_2$ with many voids. A previous study also showed that impurities in the annealing atmosphere formed voids during silicidation.[17] Therefore, we employed *in-situ* annealing inside our cobalt deposition system to produce consistent, continuous $CoSi_2$ films.

The backside sample preparation included 5 steps to reveal the $CoSi_2$/Si interface. First, the sample was bonded upside down to a glass slide of similar size for mechanical support. Epoxy Bond 110 (Ted Pella Inc.) is used for bonding the two. Thin epoxy glue was carefully applied in between and degassed, then cured at 125°C for 10 min to obtain a homogenous glue film with good adhesion.

Second, the bonded sample stack was mounted onto a specimen mount – a cylindrical Pyrex stub (Gatan Inc.) using a low-melting-point wax (Crystalbond 509, Ted Pella Inc.). The stub was heated on a hot plate at 130°C~160°C to melt a tiny granule of wax for mounting the sample stack to be ground flat. Then a metal ring (Gatan Inc.) was used to hold the stub flat on the polishing sand paper. Rough thinning of the specimen was performed with a polisher (Allied High Tech Products Inc.) until a thickness of 100 μm or less was achieved.

The thickness of the specimen was measured and monitored by the micrometer to reach the desired thickness of less than 100 μm after polishing. The Si substrate was coarsely polished sequentially by SiC sand paper of 600 grit and 1200 grit. The polished specimen was detached from the mounting stub by melting the wax on a hot plate and dissolving the remaining wax in acetone.

Third, the remaining Si substrate was removed by a heated TMAH (25 wt%) bath at 85°C. TMAH etching is highly selective towards the thermal oxide. Thus when no more bubbles were formed in the etching solution, it indicated the bulk Si had been completely removed, exposing the SiO_2 layer. Then the sample was immersed in 10:1 buffered HF solution until the SiO_2 layer of the SOI was removed, which is the fourth step.

In the final step, the remaining Si layer (~100 nm) from SOI (originally 200 nm) was removed by dry etching with XeF_2 gas. This was performed in a home-built XeF_2 etching tool. Exposed Si was quickly etched by alternating exposure to XeF_2 and subsequent pumping away of gaseous reaction products. Si reacts with XeF_2 to form gaseous Xe and SiF_4. XeF_2 etching has been used to selectively remove Si because it removes only silicon, but not photoresist, SiO_2, silicon nitride, Al, Cr, or TiN.[18] We measured that in our system the XeF_2 etch rate of $CoSi_2$ is 200 times slower than that of Si; thus XeF_2 etching can selectively remove the thin layer of residual Si. As a result of the excellent selectivity towards $CoSi_2$, the XeF_2 etching process is highly robust and tolerant towards some over-etch. This final step leaves a clean $CoSi_2$ surface, allowing the $CoSi_2$/Si interface to be examined by atomic force microscopy (AFM). The interfacial roughness study is valuable for optimizing cobalt silicide process.

Results and Discussion

We used X-ray diffraction (XRD, Bruker D8) to study cobalt silicidation process by annealing Co_xN/Si(100) structure *in*-situ at 500°C, 600°C and 700°C in N_2 for 30 sec. XRD measurements were carried out by using D8 diffractometer and 2-Dimensional detector. The as-deposited Co_xN showed a face-cubic-centered (fcc) phase, as indicated by our previous study.[13] The Co_xN remained stable in its fcc phase after RTA at 500°C. After RTA at 600°C, $CoSi_2$ with (111) and (220) orientations dominated the resulting films, while CoSi (210) and (211) orientations occurred simultaneously. This suggests polycrystalline $CoSi_2$ started to appear together with CoSi after annealing at 600°C. Meanwhile, the intensity of $CoSi_2$ (111) peak is greater than of other $CoSi_2$ and CoSi peaks, indicating that the film is textured. The CoSi completely transformed to $CoSi_2$ after RTA at 700°C, forming a textured $CoSi_2$ with a (111) preferred orientation on the Si (100) substrate. The cubic $CoSi_2$ and CoSi phases were formed directly from cubic CoN_x films without any intermediate Co-rich phases, such as tetragonal Co_2Si or orthorhombic Co_3Si at low temperatures. In a conventional Co silicide process, Co-rich silicide phases such as Co_2Si or CoSi generally formed at a low temperature ranging between 400 °C and 500 °C.[1] These results indicate that because of retardation of the Co-Si reaction by the nitrogen in the Co_xN film, the conversion of Co_xN to $CoSi_2$ does not form any intermediate Co-rich phases. This finding agrees with a previous study of $CoSi_2$ formation by annealing Co/CoN_x/Si structures.[19] Additionally, $CoSi_2$ grown by the reaction of Co_xN on Si(100) produced polycrystalline $CoSi_2$ films as expected. Although $CoSi_2$ (cubic CaF_2 structure with a = 5.36 Å) and Si (cubic diamond structure with a = 5.43 Å) have a

small lattice mismatch of only 1.2 % and similar crystallographic structure, it has proved challenging to form epitaxial $CoSi_2$ on Si substrates. Bulle-Lieuwma *et al.*[20] explained the possible reason for the polycrystalline nature of $CoSi_2$ on Si (100). They suggested that the competition between different epitaxial orientations with similar matching resulted in the growth of polycrystalline $CoSi_2$.

Figure 2 shows electron diffraction (ED) images of $CoSi_2$ from transmission electron microscopy (TEM; JEOL 2100 TEM system). ED shows that the films are polycrystalline cubic cobalt disilicide. The speckled pattern of the diffraction rings indicates that the specimen has relatively large grain sizes. The pattern showed part of the ring is more intense compared to the rest, indicating a textured film. This result agreed with the XRD result.

The resistivity of Co_xN and $CoSi_2$ thin films could be obtained by measurements of the thickness and sheet resistance. A four point probe was applied to measure the sheet resistance. The unreacted cobalt nitrides (if any) on top of the formed $CoSi_2$ were removed by a dilute sulfuric acid solution at 50 °C before the measurements. A scanning electron microscope (SEM) was used to measure the physical thicknesses. An as-deposited 30 nm Co_xN film on a Si (100) substrate generated around 120 nm of $CoSi_2$ by in-situ annealing at 700 °C (Figure 5). The formed polycrystalline $CoSi_2$ film was composed of grains and displayed thickness variation in the field of view as observed in SEM image (Figure 5b). The interfacial roughness between $CoSi_2$ film and Si substrate fabricated from CVD Co_xN is similar to that from PVD Co.[21] The resistivity of the Co_xN films decreased from 140 μΩ·cm to 20 μΩ·cm due to the formation of more conductive $CoSi_2$. This value is close to reported resistivity of $CoSi_2$, i.e. 16~20 μΩ·cm.[1]

X-ray photoelectron spectroscopy (XPS) was used to measure the composition of $CoSi_2$ films formed by annealing Co_xN on Si (100) substrates at 700°C. XPS spectra taken during argon sputtering determined the composition profiles using the Co 3p, Si 2s, C 1s, O 1s and N 1s XPS peaks. The trace of nitrogen near the surface can be attributed to a small amount of unreacted Co_xN left on the surface. Carbon and oxygen remain on the surface of the film from air exposure. The Co:Si ratio is about 1:2 inside the film. This result confirmed that we obtained cobalt disilicide with the expected stoichiometry after annealing Co_xN/Si at 700 °C.

The $CoSi_2$/Si interfacial roughness is an important factor that affects device performance. We highlight here the backside sample preparation procedure to examine the $CoSi_2$/Si interfacial roughness by AFM (Asylum MFP-3D AFM). The initial backside sample preparation was first proposed for SIMS sample preparation.[22] We adapted this method to remove the substrate and reveal the $CoSi_2$ layer of interest. The $CoSi_2$ sample was prepared by in-situ annealing Co_xN/SOI at 700 °C. We selected SOI instead of Si (100) as the substrate owing to its built-in etch-stop layer (i.e. the buried oxide of an SOI wafer). The buried oxide in SOI allowed selective removal of most of the SOI substrate.[22] We employed a combination of mechanic polishing, wet etching, and dry etching to reveal the $CoSi_2$/Si interface. Wet etching of Si-substrate is commonly performed using heated TMAH (tetramethylammonium hydroxide) or KOH solutions.[18] The wet etching is fast and easy to perform. However, the wet etching of thick and roughly polished remaining Si inadvertently leads to the formation of <111> faceted Si-pyramids. This formation of faceted Si-pyramids is caused by the highly anisotropic etch rates, with etch rates of ^{3} crystallographic orientation being 2-3 orders of magnitude lower than those of other major crystallographic orientations.[18] Therefore, wet

etching cannot be used as a high-precision polishing step, and an etch-stop layer is crucial for eliminating the roughness from the anisotropic wet-etching step. Alternatively, the Si dry etching using XeF_2 gas exhibits essentially isotropic etch rates regardless of crystallographic orientations.[18] And XeF_2 dry etching has been proved to be highly selective towards $CoSi_2$. Thus the XeF_2 dry etching process was applied to remove the thin Si remaining on top of $CoSi_2$.

To reveal and analyze the $CoSi_2$/Si interfacial morphology, we adopted a modified back-to-front sample preparation method, in which mechanical polishing, anisotropic tetramethylammonium hydroxide (TMAH) wet etching, hydrofluoric acid (HF) wet etching, and isotropic xenon difluoride (XeF_2) dry etching are employed to remove the SOI substrate from the back side to expose the $CoSi_2$/Si interface, as schematically illustrated in Figure 4. Note that for all roughness studies, "interface" is defined as the interface between $CoSi_x$ and Si, while "surface" is defined as the other side of the $CoSi_x$ film. And the surface roughness was analyzed before mounting the sample upside down onto the substrate by epoxy. Based on the AFM image and rms results shown in Figure 5 and Table 1, the CoSi formed at 600°C showed a surface roughness (10.1 nm) of 9.2 % of the silicide thickness (110 nm), and the interface roughness (13.2 nm) was 12.0 % of the silicide thickness (110 nm). When Co_xN/SOI was annealed at 700°C in N_2, stoichiometric $CoSi_2$ was formed. The surface roughness of the resulting $CoSi_2$ was determined to be around 10.3 % (12.3 nm) of the silicide thickness (120 nm), while the interface roughness is 7.6 % (9.1 nm) of the silicide thickness (120 nm). Comparing the samples annealed at 600 ^oC and 700 ^oC, the surface roughness of $CoSi_x$/Si did not change much while the $CoSi_x$/Si interfacial roughness is

substantially reduced after conversion of CoSi to $CoSi_2$ at 700°C. This is because $CoSi_2$ (cubic, lattice constant a= 5.36 Å) has a smaller lattice mismatch with Si (cubic, a= 5.54 Å), compared with CoSi (cubic, a= 4.45 Å).

Conclusions

We successfully evaluated the $CoSi_2$/Si interfacial roughness quantitatively by a backside sample preparation procedure. We obtained stoichiometric cobalt disilicide, which has low interfacial roughness because of its small lattice mismatch with Si, by *in-situ* rapid thermal annealing CVD-Co_xN at 700°C in N_2. The backside sample preparation utilized a combination of mechanical polishing, wet etching and dry etching to expose the $CoSi_2$/Si interface for AFM measurements. This approach provides a robust and reliable procedure to acquire quantitative morphological information about silicon-silicide interfaces, which can serve as an important assessment method for modern silicidation and metallization processes.

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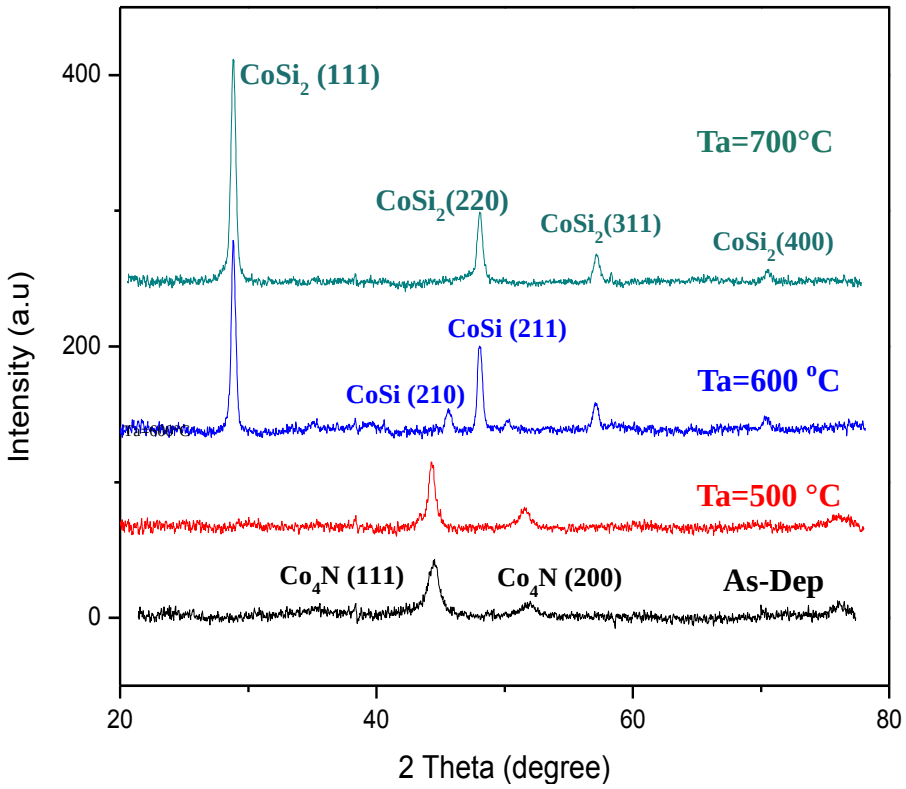

Figure 1. The XRD spectra of the as-deposited Co_xN/Si (100) and the films after *in-situ* annealing under 1 Torr of N_2 at various temperatures (T_a = 500°C, 600°C, 700°C) for 30 s.

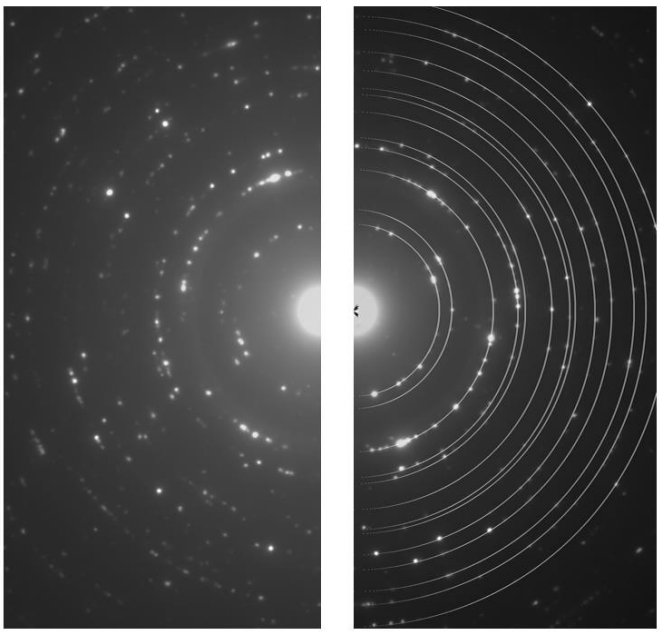

Figure 2. The electron diffraction (ED) images of $CoSi_2$ formed by *in-situ* annealing Co_xN/Si(100) in N_2 at 700°C for 30 sec.

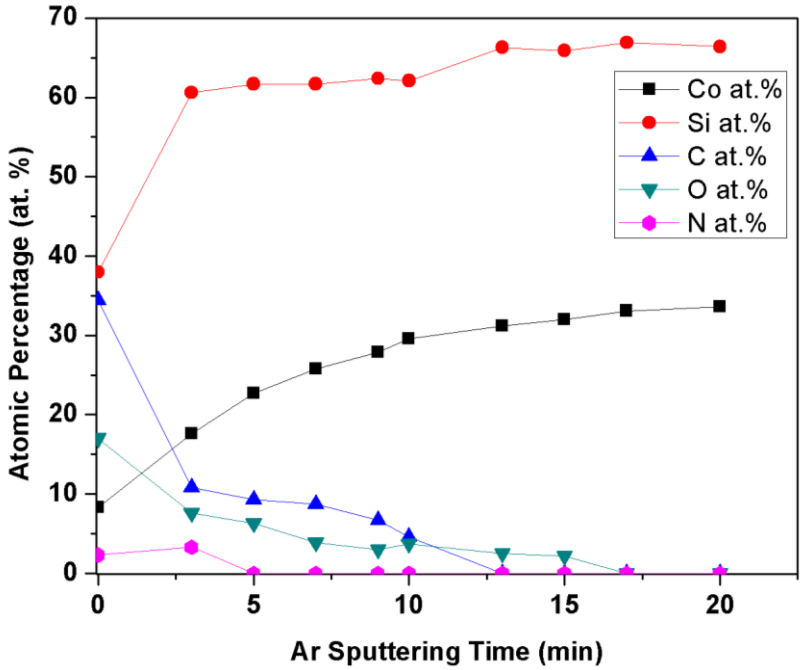

Figure 3. XPS depth-profile study of $CoSi_2$ formed by annealing Co_xN/Si (100) at 700 °C

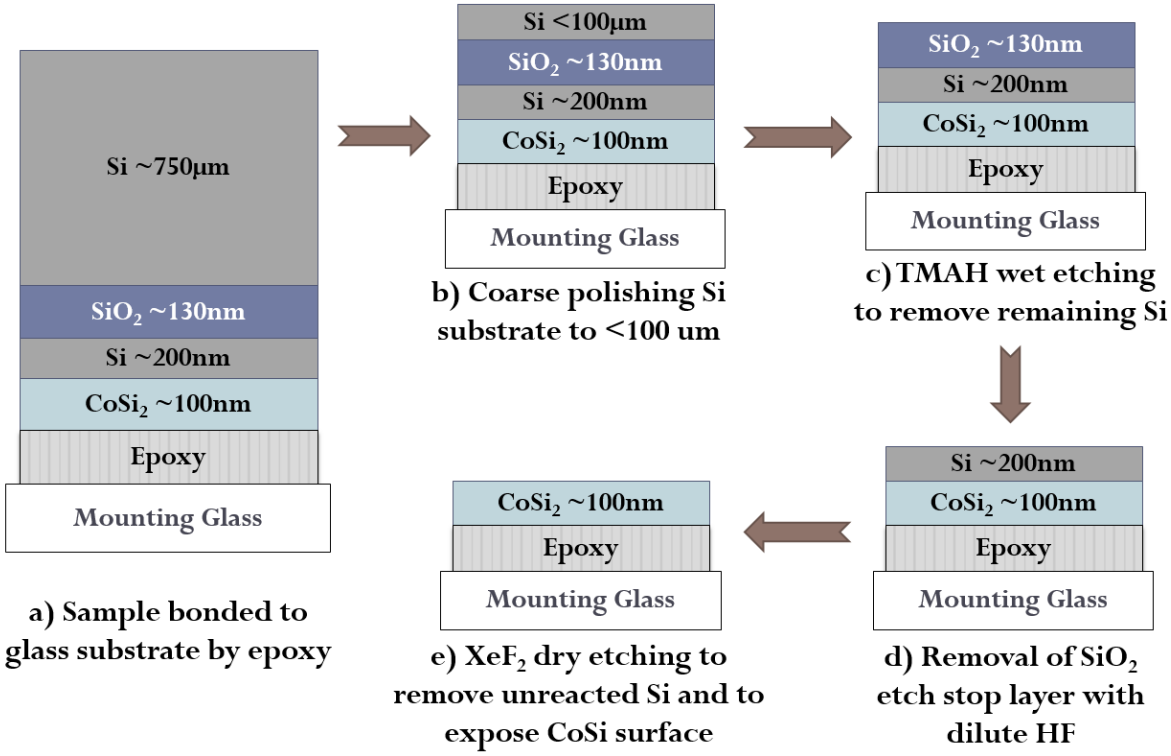

Figure 4. Schematic representation of consecutive steps in backside sample preparation procedure to reveal $CoSi_2$/Si interface: Sample is prepared by annealing Co_xN on SOI substrate at 700 °C to form $CoSi_2$ on SOI. (a) Sample is invert and fixed on a support glass substrate of approximately same size. (b) Sample after grinding the backside substrate with SiC sand paper (600 - 1200 grit) to reduce substrate thickness down to below 100 µm. (c) Sample after TMAH wet etching to selectively remove the residual silicon substrate. (d) Sample after a dilute HF etching to remove the exposed buried oxide. (e) Sample after dry XeF_2 etching to selectively remove the residual unreacted silicon, leaving the $CoSi_2$ surface ready for AFM measurements.

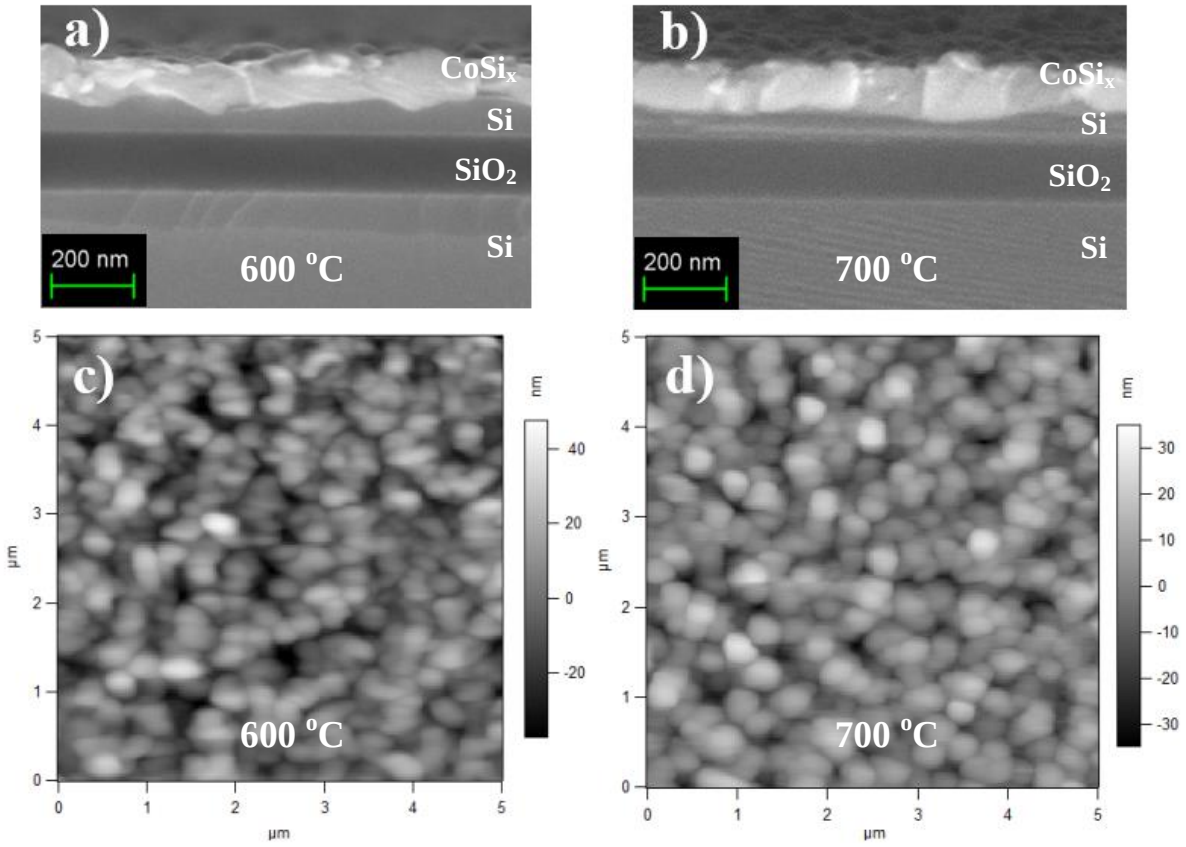

Figure 5. (a-b) Cross-section SEM images of silicided SOI substrates; (c-d) Measurement of $CoSi_2$/Si interfacial roughness by AFM. $CoSi_2$ is produced by annealing CVD Co_xN film at 700 °C in N_2.

Table 1. Cobalt silicide roughness of both surface and interface at different silicidation temperatures. Note: For roughness study, "interface" is defined as the interface between $CoSi_x$ and Si; "surface" is defined as the other side of $CoSi_x$, which was analyzed before mounting the sample upside down onto the substrate by epoxy.

Annealing Temperature (°C)	**Silicide Thickness (nm)**	**Surface Roughness**		**Interface Roughness**	
		rms (nm)	Percentage	rms (nm)	Percentage
600	**110**	**10.1**	**9.2%**	**13.2**	**12.0%**
700	**120**	**12.3**	**10.3%**	**9.1**	**7.6%**