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Direct Liquid Evaporation Chemical Vapor Deposition (DLE-CVD) of Nickel, Manganese and Copper-based Thin films for Interconnects in Three-Dimensional Microelectronic Systems

A dissertation presented

by

Kecheng Li

to

The John A. Paulson School of Engineering and Applied Sciences

in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy

in the subject of

Applied Physics

Harvard University

Cambridge, Massachusetts

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Dissertation Adviser Author

Professor Roy G. Gordon **Kecheng Li**

Direct Liquid Evaporation Chemical Vapor Deposition (DLE-CVD) of Nickel, Manganese and Copper-based Thin films for Interconnects in Three-Dimensional Microelectronic Systems

Abstract

Electrical interconnects are an intrinsic part of any electronic system. These interconnects have to perform reliably under a wide range of environmental conditions and survive stresses induced from thermal, mechanical, corrosive and electrical factors. Semiconductor technology is predominantly planar in nature, posing a severe limitation to the degree of device integrations into systems such as micro-processors or memories. 3D transistor FinFET (Fin type Field Effect Transistors) has been used by Intel since the advent of its 22 nm technology node, and has now advanced further down to 14 nm. While the technology nodes have consistently been shrinking in line with Moore's law, increasing difficulties in scaling down the feature sizes in transistors is urging the industry to seek alternative fabrication approaches for the extension of Moore's law. The most promising solution thus far is 3D heterogeneous integration, which will stack logical and analog chips together to enable multi functions chip without the need to scale the size of transistors with Moore's law. Furthermore, as wearable electronics are fast growing in the next big wave in consumer electronics after the smartphone era, interconnects face the unique challenge of having to be embedded into fashion and withstand the mechanical stresses from everyday activity. This makes the role interconnects even more important as well

as making it the main bottleneck to unleashing the full performance of the 3D microelectronics systems.

This thesis explores the fabrication, characterization and application of Nickel, Manganese, Copper based thin films for the interconnects of 3D microelectronics systems. Direct Liquid Evaporation-Chemical Vapor Deposition (DLE-CVD) technique has been proven to be a high-throughput process for high-quality Nickel, Manganese, Copper based thin films with excellent conformality in complex architectures as the interconnects for state-of-the-art 3D microelectronics systems.

Chapter 2 introduces the advantages of DLE-CVD process and its application in deposition of Nickel, Manganese and Copper based thin films. DLE-CVD process is used to deliver consistent and high vapor concentrations of Nickel, Manganese and Copper precursors to coat nanostructures with high aspect ratios.

Chapter 3 demonstrates the atom probe tomography (APT) as an effective method for understanding the 3D microstructure and compositional properties in thin films at an atomic scale. 3D compositional information of DLE-CVD NiNx, NiSi thin films from inside and outside regions of the trench structures have been investigated using APT. The APT characterization technique provides a unique tool that can be applied both to the design of 3D nanostructured microelectronic devices and to the further understanding of the fundamental physical properties.

Chapter 4 highlights the application of DLE-CVD manganese and copper based thin film process in the complex nanostructures for 3D microelectronic systems. Narrow trenches with width under 30 nm are the key nanostructure in the local interconnects in 3D FINFET with technology node smaller than 14 nm for use in microelectronic chips. It can be filled with DLE-CVD copper and copper-manganese alloy in a bottom-up fashion using a surfactant-catalyzed CVD process. An ultrathin manganese nitride layer (~ 3 nm) acts as a diffusion barrier and an adhesion layer. Through-silicon vias (TSVs) plays a crucial role in advancing the 3D integration of semiconductor devices by improving the performances of interconnections between chips. Using DLE-CVD processes, conformal, smooth and continuous copper/copper-manganese seed layers can be prepared in TSVs with aspect ratio greater than 25:1. manganese Nitride film is deposited via the DLE-CVD process to serve as an adhesion and barrier layer. Dow Chemicals achieved void-free TSV filling through the electroplating process.

Chapter 5 shows the application of the DLE-CVD manganese and copper based thin film process in the metallization of polyaramids for the application in the interconnects embedded in wearable electronic systems. Conformal and conductive coatings of copper-manganese have been successfully deposited on Kevlar fibers using the DLE-CVD process with complete film coverage. The mechanical resistance of copper-manganese coated Kevlar was tested via our in-house robotic arm system, demonstrating how the electrical resistance of the wire remains unchanged despite being flexed repeatedly to a bend of 5mm radius for half a million times.

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Kecheng Li
Cambridge, Massachusetts
May 7 2016

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To my parents

for their love and support

献给我的父亲母亲

感谢父母的爱与支持

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Chapter 1 Introduction

1.1 Interconnects in 3D Microelectronic System

1.1.1 3D Microelectronic System

Interest in three-dimensional (3D) semiconductor technology has increased dramatically in the recent years. Moore's law predicts the doubling of semiconductor transistor density every 1-1.5 years, requiring rapid advancement in device miniaturization and improvements in electrical interconnect densities. Decades of semiconductor scaling on a two-dimensional (2D) level has far outpaced innovations at the 3D die stacking technologies. As we begin to get diminishing returns in improving traditional 2D semiconductor scaling, the industry has begun focusing more on developing 3D integration with a focus on through-silicon vias (TSV) for scaling in the vertical direction and faster interconnects between multiple dies in a 3D die stack.[1]

As we progress microelectronic systems from 2D to 3D, it is important to note the dominant differences to understand the challenges that 3D systems present. 2D microelectronic systems are planar and consist of a single layer. On the other hand, 3D systems have features defined in the vertical direction and consist of multiple layers stacked together. Interconnects in the 2D

systems require films that are uniformly deposited on a flat surface that adhere well; they do not need to survive flexing of the electronic components. In the 3D systems, interconnects require films to be uniformly deposited in 3D structures with high aspect ratios, and demand that the films be capable of withstanding a large number of bends while maintaining operating performance.

1.1.2 Categories of Interconnects in 3D Microelectronic System

Through-silicon vias (TSVs), thinned silicon and fine-pitched silicon-silicon interconnections (SSIs) are the three main emerging technologies in 3D die stacks. [2] These 3D silicon technologies are rapidly gaining momentum now that Moore's law is decelerating and potentially coming to a halt. TSVs are the most promising 3D integration technology in the current strategies. [3]

TSV technology is essential for both die-to-die and wafer-to-wafer stacking in order to achieve high bandwidth and low inductance in these vertical interconnects.[4] The desired TSV structures can range widely, including diameters that range from 1 to 90 μm, with silicon thickness ranging from 1 μm typical of SOI to 730 μm which is the thickness of a full wafer. Aspect ratios of these structures can be as low as 2:1 and as high as 50:1. Copper, tungsten and other composite compounds are potential material candidates for TSVs.[5][6]

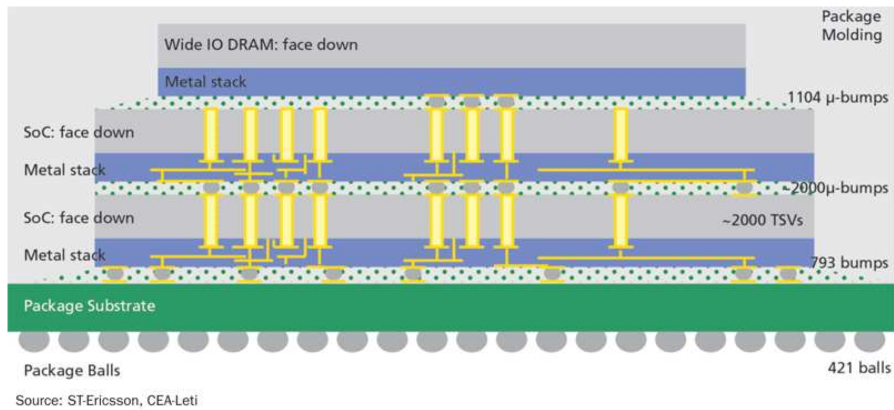


Figure 1.1. TSVs for the interconnects in 3D ICs. Source: http://www.eettaiwan.com/

The 3D transistors is a form of non-planar transistor architecture that features a gate stacked above two vertical gates, first demonstrated by Intel Corporation in September 2002. [7]With essentially triple the surface area of previous transistors for conducting electron flow, these new type of transistors allow more current to flow when they are in the "on" state, providing higher switching speed and a significantly lower power consumption. By replacing the conventional flat 2D planar gate with a thin vertical 3D fin, 3D transistors are able to provide improvements both in performance and in energy efficiency.

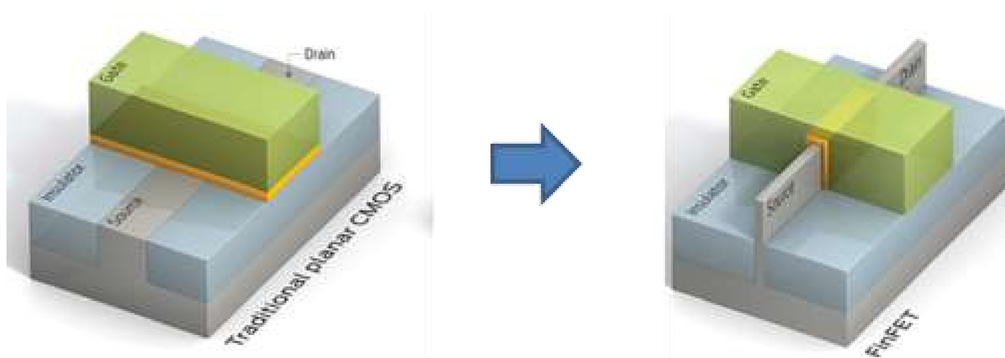


Figure 1.2. Cross-sectional micrograph view of the transistor (top) and metal interconnects (bottom)demonstrating the rate of miniaturization of in microelectronic components. Source: Intel.

Wearable electronics consists of fabric materials that are embedded with electronics connected together via interconnections, enabling smaller sizes and greater flexibilities far beyond what can be achieved using traditional manufacturing techniques for electronic systems. [8]Interconnect wires that allow the wide range of devices in the electronic systems to communicate must be sufficiently robust to survive continuous dynamic stresses brought on by flexing, bending, twisting, stretching and dropping in an uncontrolled use environment.

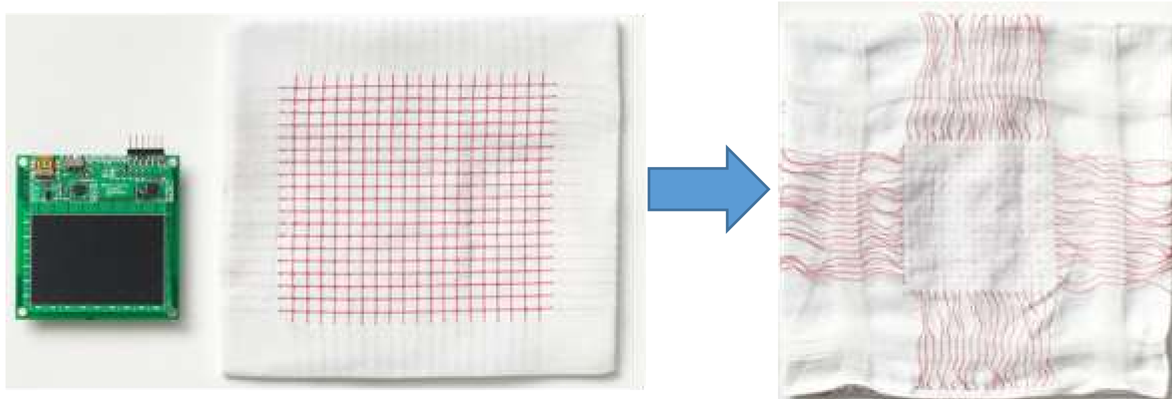


Figure 1.3. Project Jacquard makes it possible to weave touch and gesture intractivity into any textile using standard industrial looms. Source: Project Jacquard

1.2 Nickel, manganese and copper-based thin films in 3D Microelectronic System

1.2.1 Overview of Nickel, manganese and copper-based Thin Films

With the shrinking of features in microelectronic circuits, existing materials for transistor interconnects and diffusion barriers can no longer be fabricated using traditional methods involving physical vapor deposition.[9] For highly conformal thin film coatings demanded by the technological advances in the advanced semiconductor industry, new deposition processes using atomic layer deposition (ALD) and chemical vapor deposition (CVD) must be explored for compounds based on materials such as nickel, manganese and copper.[10][11]

1.2.2 Nickel-based thin Films in 3D Microelectronic System

Recent years have seen rapid miniaturization in modern electronics continue, making interfacial issues become critical for the overall performance and durability of electronic architectures, of which a most important issue is discovering a high performance contact between silicon and metals. In advanced semiconductor manufacturing processes, nickel silicide is fast becoming the preferred method for improving the contact with silicon due to its lower formation temperature, higher conductivity and smoother interface as compared to the alternatives, which are the silicide of cobalt and titanium. [12]

Although Ni silicide has various advantages, one of the greatest challenges is to reduce the silicon consumption during the silicide formation while keeping a low resistivity, low formation temperature and high stability. By introducing Ni monosilicide phase (NiSi) instead of $NiSi_2$ or

Ni_2Si, these requirements can be met since NiSi has a low resistivity of around 14 mΩ-cm and only requires formation temperature below 400 ^oC, while $NiSi_2$ requires higher than 600 ^oC and Ni_2Si is unstable when interfacing with silicon. Therefore, to enable higher-performance silicon devices, development of processes toward high-quality NiSi at Ni/Si interface is urgently called for.[13]

1.2.3 Manganese and copper-based thin Films in 3D Microelectronic System

Copper was introduced as the material of choice for interconnect lines in 1997 as a viable replacement for aluminum alloy due to copper having a lower electrical resistivity (1.67 μΩ-cm) and higher resistance towards electro migration.[14] As transistors get smaller and smaller, each new generation of microprocessors demand ever decreasing thickness of wire interconnects connecting transistors. The downscaling of these features means a reduced cross-sectional area and increased capacitance will result in the loss of device performance due to increased resistivity and increased interconnect delays (RC delays). This forced the industry to seek a higher performing replacement material for the existing aluminum-based wires.

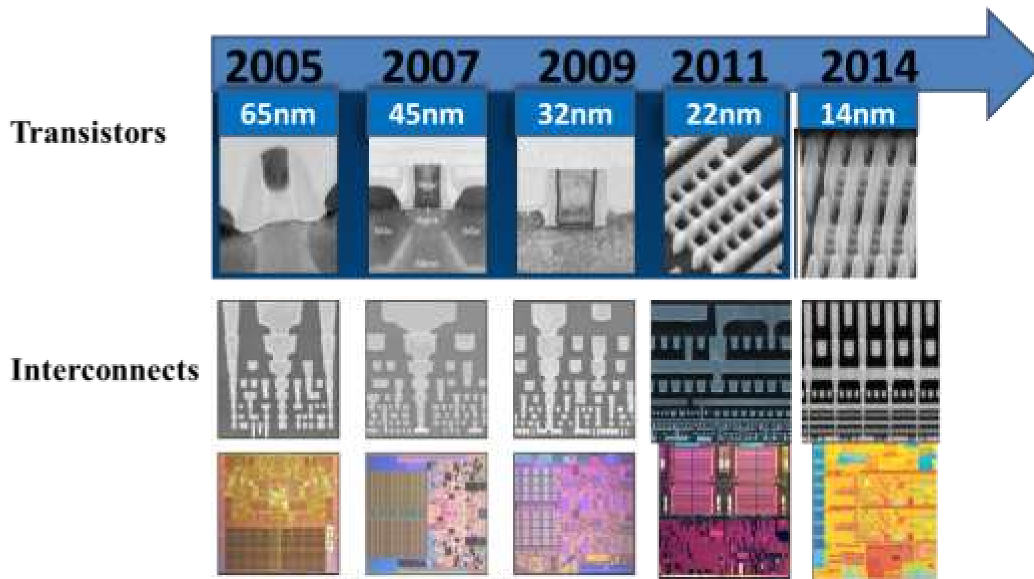


Figure 1.4. Cross-sectional micrograph view of the transistor (top) and metal interconnects (bottom) demonstrating the rate of miniaturization of in microelectronic components. Source: Intel.

When copper become the industry standard material for interconnects, it was crucial to avoid copper diffusion into the transistors as copper contamination can cause the transistors to stop functioning. As a result, diffusion barriers must be applied to the copper interconnect wires to confine them within the interconnect regions only.

Tantalum nitride diffusion barriers are typically used by the industry as a diffusion barrier material for copper.[12] Unfortunately, TaN has poor adhesion to copper, so Ta metal has to be deposited after the deposition of TaN barrier layer, followed by a thin copper seed layer and filling of the trenches and holes via electrodeposition of copper.[15]

Several challenges arise when the feature scales of these microelectronic circuits shrink dramatically in size. Due to the non-conformal characteristics of sputtered film, the sputtering of TaN as a barrier layer, Ta metal as the adhesion layer, and Cu metal as the seed layer for Cu electrodeposition are not able to provide a uniform coating in the high aspect ratio structures in these devices, resulting in film depositions that are thicker near the opening of these features and thinner near the bottom of them. Consequently, the electrodeposition of copper will fail to fill completely these trenches with high aspect ratio. Therefore highly conformal ALD and CVD thin film deposition processes have to be developed to overcome these problems.[16]

1.3 Deposition Techniques

Thin film deposition techniques are considered the most critical component to the creation of microelectronic devices. Device engineers continuously push the limits of semiconductor technologies by demanding films of higher quality and complexity, and the number of stages involved in such devices can reach over a thousand steps. The first 500 steps belong to FEOL and the remaining 500 steps correspond to the BEOL portion, both essential to the modern microprocessor fabrication.[17]

Thin film deposition is the method of choice for depositing critical layers in the nanometer to micrometer scales utilized in microelectronic devices. Thin film deposition can be classified into two different types, physical vapor deposition and chemical vapor deposition.

1.3.1 Physical Vapor Deposition

Physical vapor deposition process, unlike chemical vapor deposition processes, do not involve chemical reactions. The target material vapors are generated via thermal heating or using high energy ion bombardment. Sputtering and evaporation are the two most common techniques used in physical vapor deposition.[9]

1.3.1.1 Evaporation

During the early days of semiconductor device fabrication, the metal films were predominately deposited by evaporation technique. Wafers are inserted into a high-vacuum process chamber of the evaporator system which is evacuated by a cryogenic vacuum pump and is maintained at a low pressure of under 10^{-5} Torr. The target deposition material is heated in a crucible using an embedded resistive heater (thermal evaporation) or using a beam of electrons (e-beam evaporation). A mechanical shutter is positioned between the crucible and the substrate to allow the deposition to start and stop sharply and abruptly. Under such low pressure in the chamber, the material vapors transverse across the chamber in a straight path before arriving at the surface of the substrate wafer. Over time the accumulation of material vapors on the substrate results in the formation of the desired film.[18]

1.3.1.2 Sputtering

Sputtering is the primary deposition technique used to deposit diffusion barriers, adhesion layers and seed layers in copper interconnect systems. Sputtering involves ejecting particles of the target material to be deposited from a solid target material using the energetic bombardment of this target using high energy particles just as inert gas ions.[9]

In a sputtering system, the plasma chamber is designed so that high-energy ions striking the solid target material. The higher pressure in sputtering systems results in films of higher conformity and step coverage due to atoms experiencing more gas-phase collisions. Material

composition can be controlled more closely and deposition rates can be high. With sputtering being a physical etching process, a wide range of materials are suitable for deposition using the sputtering technique. When high growth rates are desired, DC sputtering is employed. On the other hand, when the deposited materials are insulating in nature, RF sputtering involving plasma is preferred.[19]

1.3.2 Chemical Vapor Deposition

Chemical vapor deposition is the process of reacting the vapor of a volatile precursor compound with other gases via chemical reactions, to produce high quality, high-performance nonvolatile solid film that deposits on a substrate. [17] Volatile by-products are usually produced from the CVD reactions, which are evacuated from the process chamber by gas flows. CVD methods are often used in the semiconductor industries to deposit a large range of thin films.

CVD is a popular technique compared to other vacuum deposition methods due to its low equipment costs and affordable operating expenses for films and coatings of metals, insulators and semiconductors. CVD is able to deposit materials in various morphologies, such as epitaxial, polycrystalline and amorphous films. Furthermore CVD processes have the unique capabilities to enable surface-selective deposition and uniformly coat structures with very high aspect ratios.[10][20]

There are 3 main formats of CVD each operating at a different pressure. Atmospheric pressure CVD (APCVD) is a variant of CVD that deposits at atmospheric pressure. Low-pressure CVD (LPCVD) operates at sub-atmospheric pressures in the range of 5-20 Torr to reduce unwanted reactions in the gas-phase and for increased film uniformity across the wafer substrates. Ultrahigh vacuum CVD (UHVCVD) is CVD that operates at very low pressure, often in the order of 10^{-8} Torr. Plasma-Enhanced CVD (PECVD) enhances the rate of CVD reactions at lower temperatures by placing the substrate in the plasma discharge region.[10]

1.3.3 Direct Liquid Evaporation Chemical Vapor Deposition

Direct liquid evaporation chemical vapor deposition (DLE-CVD) is a promising and attractive deposition technique that has widespread applications to a large variety of pressures and is especially effective in leveraging CVD precursors having low vapor pressures. [21]

Organometallic CVD precursors typically have low vapor pressures of under 1 Torr at room temperature but high vapor pressures are needed to deposit high quality films with high conformity and high growth rates. However, the high temperatures needed to achieve sufficient vapor pressures for use with conventional CVD bubblers can result in thermal decomposition of those precursors that lack the necessary thermal stability. This gives rise to the incorporation of impurities in the film as well as non-uniformity in the deposited films.

DLE-CVD solves the challenging problem of avoiding premature thermal decomposition when using precursors with low vapor pressures at elevated temperatures. In a DLE-CVD setup, the

CVD precursor is dissolved in a solvent that is chemically insert. Small amounts of liquid are precisely delivered into a long heated spiral length of vaporizer tubing for full vaporization of the liquid droplets. A carrier gas is used to transport these vaporized chemicals for mixing with the co-reactants before they are injected into the reaction chamber for deposition on the substrate.[13]

1.4 Overview of Thin Film Characterization

1.4.1 Thickness and Structural Characterization

Atomic force microscopy (AFM) is used to investigate the surface morphology of thin films. It is a ultra-high resolution variant of the scanning probe microscopy (SPM) with sub-nanometer resolution. The AFM system has a tiny and sharp mechanical probe that measures the forces acting between this probe and the surface of the sample being measured using the reflection of a laser spot off the top surface of the AFM cantilever tip.[22]

Scanning electron microscopy (SEM) is used to measure the thickness of thin films with thicknesses that are much larger than tens of nanometers, to analyze the surface morphology of the films as well as to inspect the step coverage of thin films on high aspect ratio (AR) features. SEM is a variant of the electron microscope that injects a focused beam of electrons at the surface of the sample, and measures how the incident electrons interact with the atoms on sample's surface, giving us high-resolution images of the sample's surface topology, electrical resistivity and composition. SEM is commonly employed for both top-view and cross-sectional analyses due to the ease of their sample preparation.[23]

Transmission electron microscopy (TEM) is a ultra-high resolution electron microscopy technique. TEM is similar to SEM in many ways, and it shoots a beam of electrons through an ultra-thin sample that has been specially prepared to this thickness. The electrons interact with the specimen producing an image with resolution with an order of magnitude higher than that

of the SEM. This image is projected onto an imaging device such as a CCD camera. There are two main methods of preparing a sample for cross-sectional TEM analysis.[24] The first method involves placing 2 identical samples together facing each other mechanical polishing to thin them down, followed by ion milling to the desired thickness that is transparent to the incoming electron beam. The second method involves using the focused ion beam (FOB) where the target region to be extracted is coated with a layer of protecting material, after which a wedge of the material is milled out using the FIB system.[25] This FIB'ed wedge is then held in place on a TEM grid with a thin layer of metal deposition. Finally, the wedged sample is thinned further to about a micron in thickness.

1.4.2 Chemical Characterization

X-ray photoelectron spectroscopy (XPS) is a surface analysis spectroscopic technique that measures the elemental composition, chemical state, empirical formula and electronic state of the elements in a specimen. A beam X-rays is generated and focused on a micro-sized spot on the sample being measured. The irradiated x-ray excites the electrons in the various orbitals of the material, causing some electrons to be excited and emitted from the surface of the materials as photoelectrons. The photoelectrons are then collected by a detector where the kinetic energies of the collected particles are measured, producing the XPS spectrum. Since we know the energy of a particular X-ray wavelength (E_{photon}), we are able to calculate the binding energy of these electrons

$$E_{binding} = E_{photon} - (E_{kinetic} + \phi)$$

where $E_{kinetic}$ is the kinetic energy of the photo electron measured by the XPS detector, and ϕ is the work function of the spectrometer.[26]

Rutherford backscattering spectroscopy (RBS) is a characterization technique that is used to determine the structure and composition of thin films by impinging a beam of high energy ions on the specimen and measuring the backscattering of this beam. Rutherford backscattering involves the elastic collision of a high kinetic energy particle from the incident beam to a stationary particle on the sample. By the law of conservation of energy and momentum, the energy E_1 of the backscattered projectile is reduced from the initial energy E_0:[27]

$$E_1 = k.E_0$$

where k is the kinematic factor

$$k = \left(\frac{m1cos\theta \pm \sqrt{m_2^2 - m_1^2(sin\theta_1)^2}}{m1 + m2} \right)^2$$

Energy-dispersive X-ray spectroscopy (EDX) is a characterization technique for doing elemental analysis or chemical characterization of a sample. It uses a high-energy beam of electrons, protons or X-rays to excite an electron in the ground state in an inner shell, ejecting it to create an electron hole pair.[28] This causes a higher energy in an outer, higher energy shell to relax down to fill the newly created hole. This difference in energy between the higher energy shell

and the lower energy shell may result in the emission of X-rays, which are measured by an energy-dispersive spectrometer and the elemental composition of the sample is determined based on how energies of X-rays are characteristic of the difference in energy between the two shells and the specimen’s atomic structure.

1.4.3 Atom Probe Tomography

1.4.3.1 Unique features of the Atom Probe Tomography

Atom Probe Tomography (APT) is an extremely high resolution analysis technique for characterizing materials, providing unique data in both the atomic structure and the chemical composition of the specimen, making APT a highly complementary technique to the various forms of electron microscopy. APT has the unique ability to construct three-dimensional models of the chemical composition of the specimen at an atomic scale, with a resolution of under 3 angstroms in all 3 dimensions with an analytical sensitivity of up to 10 ppm. This makes APT an excellent method to investigate features located beneath the surface of the specimen, not limited to dislocations, two-dimensional features (including interfaces and layered structures) and three-dimensional features (such as precipitates).[29]

In addition to its unmatched spatial resolution and high analytical sensitivity, APT poses several distinct advantages not seen in other analytical instruments. The detection efficiency of APT is very high at over 50%. It is also capable of detecting all elements with the same efficiency due

to having a time-of-flight (TOF) mass spectrometer and microchannel plates (MCPs) being equally sensitive to all elements. Furthermore, no prior knowledge of the composition is needed.[29]

1.4.3.2 Fundamentals of the Atom Probe Tomography

Field evaporation is the effect exploited by APT where a very strong electric field is applied to the specimen for the field-induced removal of atoms from the specimen's surface. This electric field, created using either a standing (DC) electrostatic field combined with either a high voltage (HV) field or a sequence of laser pulses, is able to ionize the surface atoms with single or multiple charges causing it to desorb from the surface.[29]

The removed ions are pulled towards a reflection compensator configuration which straightens the curved trajectory of these ions towards a position-sensitive detector, which collects them and measures their impact positions. TOF measurements of individual ions are made possible due to the pulsing of the high voltages or laser pulses, which is used to determine the mass to charge ratio for the identification of the elements corresponding to each collected ions. These processes can be seen schematically in Figure 1.5

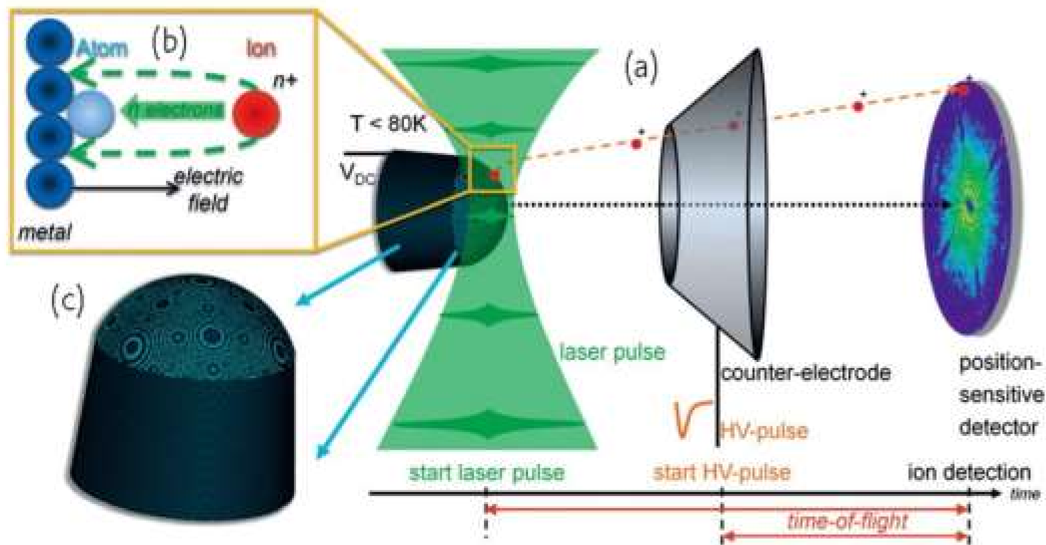


Figure 1.5 (a) Schematics of the atom probe tomography process. (b) An illustration of the field evaporation process. (c) An example of a 3D representation of the specimen. The regions shaded in light blue represent atoms protruding from the specimen, and these patterns represent the crystal structure of the specimen. [29]

Before the specimen is ready for field evaporation of surface atoms, it must first be sharpened into a sharp tip with a radius of curvature between 50 to 150 nm as well as a sharp shank angle of usually under 20 degrees in order to achieve the desired evaporation field. The surface electric field can be estimated with

$$F = \frac{V}{k_f R}$$

where F is the induced electric field at the apex of the sharpened tip, R is the radius of curvature of this tip, k_f is the field factor which is also known as the field reduction factor (a constant that is characteristic of the shape of the tip and the electrostatic environment the tip resides in).

The cone shape geometry of the sharpened tip allows a highly magnified projection in the order of 10^6 using the resulting highly divergent electric field. This allows atoms 0.2 nm apart on the surface of the specimen to strike the detector with a separation of 0.2 mm, allowing this measurement to be made with high precision and ease. Furthermore, the specimen is cooled down to cryogenic temperatures to reduce surface diffusion of the specimen's atoms, increasing the spatial resolution even more. A reverse-projection algorithm is used to reconstruct a 3D atomically resolved tomographic structure of the analyzed volume of the specimen using the positions of the atoms collected by the detector.[29]

APT is able to operate using either HV pulses or laser pulses. Using HV pulses involve an electric field created from the combination of a standing DC voltage and HV pulses. This requires the specimen to be sufficiently conductive (with a electrical conductivity greater than 10^2 S cm^4). As a result, this limits the use of HV pulses to typically metallic samples. Optimizations have to be made for the standing voltage, the specimen temperature and the pulse fraction for each specimen such that there is no preferential evaporation of the elements experiencing the lowest electric field and simultaneously avoid the evaporation of atoms by field evaporation due to just the standing voltage only. The pulse fraction is defined as the ratio of the HV pulse amplitude to the DC standing voltage.[29]

The alternative pulsing mode is the laser pulsing mode. This method uses laser pulses in the picosecond and femtosecond ranges for inducing field evaporation on the apex of the specimen

tip. Unlike the HV pulses, laser pulses allow insulating materials to be analyzed without too many specimen failures. This makes it suitable for characterizing specimens comprised of semiconductors, organic compounds, ceramics and bio minerals. Because the energy of laser pulses is hard to vary compared to the pulse duration, the pulse fraction is varied as the DC voltage changes, as opposed to the case of the HV-pulsing mode.[30]

APT exercises very precise control over the pulsed field evaporation by having tight control over the HV and laser pulsing. This enables it to accurately control the precise moment an ion is ejected from the surface of the tip, allowing the instrument to measure the TOF of the ion, defined as the time between the pulse application and the time the ejected particle is measured by the detector. The mass-to-charge ratio m/n of the ion is related to the TOF by the formula

$$\frac{m}{n} = \frac{2eV}{v^2} = \frac{2eV}{d^2}t^2$$

Where *m* is the mass of the atom, *v = d/t* is the velocity of the atom, *d* is the distance o separation between the specimen and the detector, and *t* is the time of flight. The potential energy of the surface atom due to the electric field, neV, is convered to kinetic energy $\frac{1}{2}mv^2$.[30]

The highly accurate measurement of the TOF of the evaporated atoms allows for the elemental identification of these detected ions. Coupled with the location data of each detected ions, the

final compositional mapping of the specimen volume can be reconstructed in 3-dimensions with atomic scale resolution using APT.

1.4.3.3 Limitations of the Atom Probe Tomography

APT analysis requires tremendous skill and experience to operate as the number of successful specimen runs is highly dependent on it. Fracturing of specimen is a typical problem during APT analysis. This can be a result of the high mechanical stresses on the specimen at the apex region when they approach the cohesive strength of the material. This prevents sufficient data to be collected during the experiment. The efficiency of ion collections is greatly limited to under 60% of incident atoms due to the area on the MCPs that are open for them. Specimens with complex structures also serve to be challenging as a high degree of distortion can be introduced into the 3D reconstructed images. The volume being analyzed is also limited by the field of view of the spatial detector, resulting in data sets 100 nm in diameter and 100 nm in depth, which gives a volume of 10^6 nm^3 and 10^7-10^8 atoms. Such a run will require 17 hours of collection time based on an optimistic collection rate of 10^6 atoms/min.[31]

Table 1.1. Summary of Major Chemical Characterization Techniques

Method	Primary Beam	Detected Signals	Elemental Sensitivity	Detection Limit	Lateral Resolution	Effective Probe Depth
APT/APM	-	Ions	H-U	~ few ppm	0.3 – 0.5 nm	~ 1 – 3 Å
EDS	Electron	Characteristic X-ray	Na –U	~ 0.1%	~ 1 µm	~ 1 µm
RBS	He+ ions	Backscattered ions	He-U	~ 0.1%	~ 1 µm	~ 4 µm
SIMS	Cs^+, O_2^- ions	Secondary ions	H-U	> 0.1 ppm	~ 1 µm	~ 15 Å
XPS	X-ray or UV	Photoelectrons	Li-U	~ 0.1 – 1%	~ 100 µm	5 - 15 Å
XRD	X-ray	Diffracted X-ray	Crystalline Material	5%	> 1 µm	> 1 µm

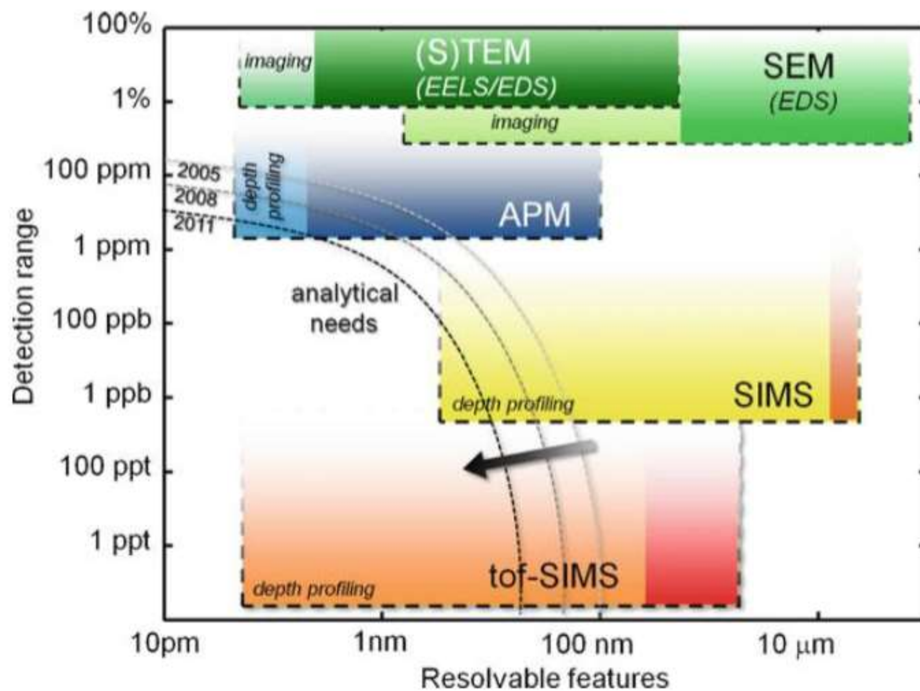


Figure 1.6. Typical elemental sensitivity (detection range) and sparial resolution of common microscopy and microanalysis techniques. The dotted lines indicate imaging techniques ((S)TEM, SEM) or depth profiling (SIMS, APM). [30]

Reference

[1] S. Arpiainen, *Integration of 2D and 3D nanostructure fabrication with wafer-scale microelectronics Photonic crystals and graphene Integration of 2D and 3D nanostructure fabrication with wafer-scale microelectronics Photonic crystals and graphene*. .

[2] J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, C. S. Patel, R. J. Polastre, K. Sakuma, E. S. Sprogis, C. K. Tsang, B. C. Webb, and S. L. Wright, “3D silicon integration,” *Proc. - Electron. Components Technol. Conf.*, no. December, pp. 538–543, 2008.

[3] T. Wafers, F. Flip, and C. Applications, “(12 > Ulllted States Patent USING THROUGH SILICON VIAS AND,” vol. 2, no. 16, 2005.

[4] J. Q. Lu, “3-D hyperintegration and packaging technologies for micro-nano systems,” *Proc. IEEE*, vol. 97, no. 1, pp. 18–30, 2009.

[5] Y. Au, Q. Min Wang, H. Li, J.-S. M. Lehn, D. V. Shenai, and R. G. Gordon, “Vapor Deposition of Highly Conformal Copper Seed Layers for Plating Through-Silicon Vias (TSVs),” *J. Electrochem. Soc.*, vol. 159, no. 6, p. D382, 2012.

[6] C. Krauss, S. Labat, S. Escoubas, O. Thomas, S. Carniello, J. Teva, and F. Schrank, “Stress measurements in tungsten coated through silicon vias for 3D integration,” *Thin Solid Films*, vol. 530, pp. 91–95, 2013.

[7] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, F. Jeffrey Bokor, and C. Hu, “FinFET-A self-aligned double-gate MOSFET scalable to 20 nm,” *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, 2000.

[8] M. Stoppa and A. Chiolerio, “Wearable electronics and smart textiles: A critical review,” *Sensors (Switzerland)*, vol. 14, no. 7, pp. 11957–11992, 2014.

[9] J. Singh, F. Quli, D. E. Wolfe, and J. Schriempf, “An Overview: Electron Beam-Physical Vapor Deposition Technology-Present and Future Applications,” *Surf. Eng. Sci. Technol. I*, pp. 59–74, 1999.

[10] A. C. Jones and M. L. Hitchman, “Overview of Chemical Vapour Deposition,” *Chem. Vap. Depos. Precursors, Process. Appl.*, pp. 1–36, 2009.

[11] Y. Au, Y. Lin, and R. G. Gordon, “Filling Narrow Trenches by Iodine-Catalyzed CVD of Copper and Manganese on Manganese Nitride Barrier/Adhesion Layers,” *J. Electrochem. Soc.*, vol. 158, no. 5, p. D248, 2011.

[12] M. Tinani, a. Mueller, Y. Gao, E. a. Irene, Y. Z. Hu, and S. P. Tay, “In situ real-time studies of nickel silicide phase formation,” *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 19, no. 2, p. 376, 2001.

[13] Z. Li, R. G. Gordon, H. Li, D. V. Shenai, and C. Lavoie, “Formation of Nickel Silicide from Direct-Liquid-Injection Chemical-Vapor-Deposited Nickel Nitride Films,” *J. Electrochem. Soc.*, vol. 157, no. 6, p. H679, 2010.

[14] R. Civanlar, A. Eleftheriadis, and O. Shapiro, “United States Patent,” 2009.

[15] K. I. Choi, B. H. Kim, S. W. Lee, J. M. Lee, W. S. Song, G. H. Choi, U. Chung, and J. T. Moon, “Characteristics of ALD-TaN Thin Films Using,” *Ieee*, pp. 129–131, 2003.

[16] Z. Li, A. Rahtu, and R. G. Gordon, “Atomic Layer Deposition of Ultrathin Copper Metal Films from a Liquid Copper(I) Amidinate Precursor,” *J. Electrochem. Soc.*, vol. 153, no. 11, p. C787, 2006.

[17] R. Gordon and J. Becker, “Vapor deposition of metal oxides and silicates: Possible gate insulators for future microelectronics,” *Chem. …*, no. 12, pp. 2463–2464, 2001.
[18] N. Kaiser, “Review of the fundamentals of thin-film growth.,” *Appl. Opt.*, vol. 41, no. 16, pp. 3053–3060, 2002.
[19] J. A. Thornton, “Magnetron sputtering: basic physics and application to cylindrical magnetrons,” *J. Vac. Sci. Technol.*, vol. 15, no. 2, pp. 171–177, 1978.
[20] B. Potts and P. Mark, “(12) Ulllted States Patent (10) Patent N0 .: ( ) Nonce : Assistant Examiner * Anshu Bhatia US . Patent,” vol. 1, no. 12, pp. 1–7, 2013.
[21] T. Zumin, “United States Patent [19],” pp. 1–5, 1980.
[22] G. Binnig and C. F. Quate, “Atomic Force Microscope,” *Phys. Rev. Lett.*, vol. 56, no. 9, pp. 930–933, 1986.
[23] T. Hideo and T. Otaka, “Scanning Electron Microscope,” 1995.
[24] H. P. Stevenson, A. M. Makhov, M. Calero, A. L. Edwards, O. B. Zeldin, I. I. Mathews, G. Lin, C. O. Barnes, H. Santamaria, T. M. Ross, S. M. Soltis, C. Khosla, V. Nagarajan, J. F. Conway, A. E. Cohen, and G. Calero, “Use of transmission electron microscopy to identify nanocrystals of challenging protein targets.,” *Proc. Natl. Acad. Sci. U. S. A.*, vol. 111, no. 23, pp. 8470–5, 2014.
[25] K. Kuroda, “Application of focused ion beam milling to cross-sectional TEM specimen preparation of industrial materials including heterointerfaces,” *Thin Solid Films*, vol. 319, no. 1–2, pp. 92–96, 1998.
[26] D. D. Sarma, P. K. Santra, S. Mukherjee, and A. Nag, “X-Ray Photoelectron Spectroscopy : A Unique Tool to Determine the Internal Heterostructure of Nanoparticles X-Ray Photoelectron Spectroscopy : A Unique Tool to Determine the Internal Heterostructure of Nanoparticles,” 2013.
[27] H. Hashimoto, A. Ohno, K. Nakajima, M. Suzuki, H. Tsuji, and K. Kimura, “Surface characterization of imidazolium ionic liquids by high-resolution Rutherford backscattering spectroscopy and X-ray photoelectron spectroscopy,” *Surf. Sci.*, vol. 604, no. 3–4, pp. 464–469, 2010.
[28] D. Nam, A. S. Opanasyuk, P. V. Koval, A. G. Ponomarev, A. R. Jeong, G. Y. Kim, W. Jo, and H. Cheong, “Composition variations in Cu2ZnSnSe4 thin films analyzed by X-ray diffraction, energy dispersive X-ray spectroscopy, particle induced X-ray emission, photoluminescence, and Raman spectroscopy,” *Thin Solid Films*, vol. 562, pp. 109–113, 2014.
[29] M. K. Miller, D. Larson, T. Prosa, R. Ulfig, B. Geiser, T. Kelly, and Imago, *Atom Probe Microscopy*, vol. 10, no. S02. 2013.
[30] D. Larson, T. Prosa, R. Ulfig, B. Geiser, and T. Kelly, Local electrode atom probe tomography. 2013.
[31] E. a. Marquis, “Atom probe tomography applied to the analysis of irradiated microstructures,” J. Mater. Res., vol. 30, no. 09, pp. 1222–1230, 2015.

Chapter 2 DLE-CVD Processes of nickel, manganese and copper-based thin films

2.1 Introduction

Direct liquid evaporation (DLE) is a very attractive deposition method, which can be applied to a wide range of precursors, especially ones that have low vapor pressure. DLE of suitable liquids or solutions can consistently deliver high vapor concentrations of precursors that are very difficult to achieve by the typical method involving vaporization of precursors from conventional bubblers.[32] Higher vapor concentrations enable the deposition of highly conformal films with high growth rates. In this chapter, DLE-CVD is used to deliver consistent and high vapor concentrations of nickel, manganese and copper precursors to coat structures with high aspect ratios for use in next-generation microelectronics interconnect applications.

Nickel nitride, manganese nitride and copper have been previously deposited by various means, including PVD, CVD and ALD methods.[13] As the advancement of microelectronic devices demands the rapid shrinkage of features in devices, highly conformal metal deposition is required for the ultra large scale integration (ULSI) fabrication of three dimensional structures. [33] The poor step coverage of PVD methods caused severe limitations in coating deep contact holes and ultra-small trenches. [34]CVD and ALD are thus ideal deposition methods for these devices as they are able to produce high-quality and conformal thin films that meet the high demands of these advanced semiconductor devices. [17]

The thermal ALD NiNx process uses bis(*N,N'*-di-*tert*-butyl-acetamidinato)nickel(II) as the metal precursor and H_2 and NH_3 as the co-reactants, respectively. Successful depositions of high quality NiN_x and Ni metal films have been achieved. The CVD process uses bis(*N,N'*-diisopropylpentylamidinato) manganese (II) as the metal precursor and NH_3 as the co-reactant, achieving successful deposition of high quality manganese nitride at temperatures as low as 130°C. High quality copper films can also be achieved by CVD process with copper (*N,N'*-di-*sec*-butylacetamidinate) dimer as the precursor and H_2 as the co-reactant. [35][36]

However, the growth rate of Ni metal using either ALD or CVD is too slow for many practical applications. In contrast, direct-liquid-injection (DLI-CVD) process provides a much faster growth rate. It has the advantage of being able to prevent early decomposition of the precursors compared to the traditional bubbler delivery since the precursor solution for a DLI-CVD system is typically stored at room temperature.[32] Furthermore, this technique can be applied to a wide range of precursors, especially for those having low vapor pressure and limited thermal stability. DLI-CVD can deliver high vapor concentration of precursors that are challenging conventional bubbler delivery to achieve, making it favorable for growing highly conformal films with high growth rates. DLI-CVD has been successfully employed for the deposition of Ni, Co, cobalt oxide, Ru, Cu and metal oxides. [32][13][5]The DLI-CVD method typically uses a nebulizer to break up the liquid solution into tiny droplets, which then generate vapor when the droplets are exposed to a hot carrier gas. However, the process still has obstacles to be widely used in the industry, since it produces small particles made up of non-volatile residues in the precursor after most of the precursor has evaporated. These particles

can be carried along with the vapor into the deposition region, where they can contaminate substrates. Particle contamination is a very serious problem in microelectronics manufacture industry. Particles can cause defects for thin film materials; also, they can accumulate in the narrow openings of nebulizer or block the liquid flow. [32]

We developed a direct-liquid-evaporation (DLE-CVD) process to avoid the obstacles of the DLI-CVD process. DLE vaporizes the precursor solution by flowing the liquid along the heated tubing coil inside the oven. It takes advantage of the faster heat transfer from a heated solid tube to the flowing liquid than the slower heat transfer from the heated carrier gas to the liquid droplets. Even if any non-volatile residue is left behind by DLE process, the residue tends to adhere to the bottom of the tube where it remains instead of being carried into the reactor. The tubing does not become clogged or blocked. Our DLE systems have demonstrated steady, reproducible performance for years without the need to replace the tubing oils.

The choice of a suitable precursor and its solvent is crucial for obtaining high quality films via the DLE-CVD process. The precursor requires a reasonable volatility and high decomposition temperatures.[32][13][37] Both the solubility of precursor and vaporization rate is crucial when deciding on a suitable solvent. The solubility of precursor should be high enough in the solvent to ensure a sufficient supply of precursor during the deposition. The vaporization rate of solvent must be similar to that of the precursor; if the solvent evaporates more quickly than the solid precursor, the precursor residue will block the vaporizer. In this chapter, bis(*N,N'*-di-*tert*-butyl-acetamidinato)nickel(II), copper (*N,N'*-di-*sec*-butylacetamidinate) dimer, bis(*N, N'*-di-*tert*-

butyl-acetamidinato)manganese(II) are selected as the precursors for nickel, manganese, copper based thin film deposition. Tetradecane and trihexyamine are chosen for the solvents. We investigated the impact of different processing parameters and found optimal conditions for producing highly-conformal, high-quality nickel, manganese and copper-based thin films using DLE-CVD processes.

2.2 Experiments

2.2.1 Metal Amidinate Precursors

CVD and ALD precursors need to be highly reactive toward the surfaces of substrates and to the surface prepared by a complementary precursor such as H_2O, NH_3, or H_2. These compounds must also be volatile and thermally stable at the desired growth temperatures, and the reaction byproducts should be nonreactive and noncorrosive. CVD precursor chemistry has been dominated by halides, alkoxides, β-diketonates, alkyls, and cyclopentadienyl derivatives. [38] Alkylamide precursors have attracted more attention in recent years because these compounds do not have M-C bonds, resulting in minimal carbon incorporation in the deposited films, and the lower M-N bond strengths as compared to those of the M-Cl and M-O bonds allow depositions to occur at relatively low temperatures. These amide derivatives produce no corrosive byproducts, unlike metal halides. Metal amidinates are alternatives to alkylamides. [39] The amidinate ligand can provide volatile metal amidinate compounds. The bidentate chelating effect, on the other hand, should increase the thermal stability of resulting metal

compounds. In this thesis, we study the DLE-CVD of nickel, manganese and copper thin films using metal amidinates precursor.

2.2.2Precursor Chemistry in DLE-CVD of nickel, manganese and copper-based thin film

The Nickel precursor

The nickel precursor, bis(*N,N*′-di-*tert*-butylacetamidinato)nickel(II) [38] ,is a dark brown, air-sensitive crystalline solid that melts at a temperature of 87 ^{o}C. This liquid precursor has a vapor pressure of ~200 mTorr at 90 ^{o}C and ~320 mTorr at 120 ^{o}C.

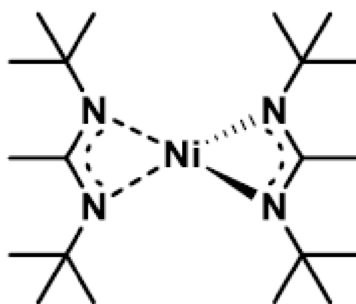


Fig 2.1. bis(N,N′-di-tert-butylacetamidinato)nickel(II) Molecular Structure

The Manganese Precursor

The manganese precursor, bis(*N,N*′-di-*tert*-butylacetamidinato)manganese(II)[38], is a dark yellow, super air-sensitive crystalline solid that melts at a temperature of 106 ^{o}C. This liquid precursor has a vapor pressure of ~52 mTorr at 100 ^{o}C

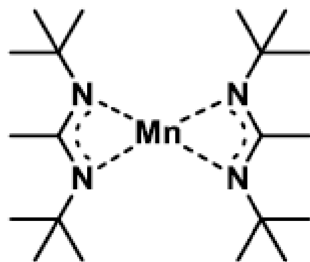


Fig 2.2. bis(N,N′-di-tert-butylacetamidinato)manganese(II) Molecular Structure

The Copper Precursor

The copper precursor, copper (*N,N′*-di-*sec*-butylacetamidinate) dimer[35] is bright white, air sensitive crystalline solid that melts at a temperature of 75 ^{o}C. The liquid precursor has a vapor pressure of ~187.5 mTorr at 95 ^{o}C.

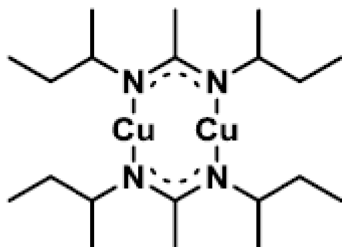


Fig 2.3. Copper (N,N′-di-sec-butylacetamidinate) dimer Molecular Structure

2.2.3 Choices of Solvents

There are several requirements for choosing the solvent:[37]

1. The solvent should be inert. The precursors must be soluble and stable for long periods in the specific solvent, and must not react with the solvent.
2. The solvent should have a vapor pressure similar to the precursor

3. In the case of ternary oxides, as multiple precursors co-exist in the solvent they should not react with each other. Co-precursors should evaporate at similar temperatures. Otherwise it will be difficult to control the composition of complex oxides.

In this paper, trihexylamine and tetradecane are chosen as the solvent of copper, manganese, Nickle precursors. In Fig. 2.5, The Thermal Gravimetric Analysis (TGA) of copper, manganese amidinate and Trihexylamine shows their volatilities are quite similar.

Trihexylamine Boiling Point 265 °C   Tetradecane Boiling point 253 °C

Fig2.4. The Molecular Structure of Trihexylamine and Tetradecane

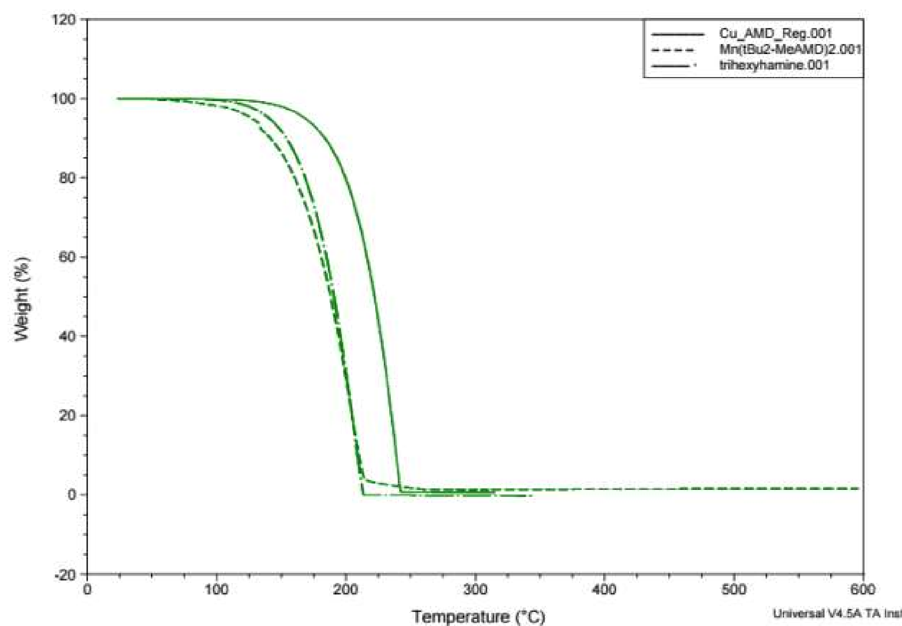


Figure 2.5. Thermal Gravimetric Analyses of Cu and Mn amidinates and Trihexylamine

The nickel, manganese and copper precursor solutions were prepared in a glovebox. The precursor solution is finally transferred into containers inside the glove box. Manganese and copper precursors were then injected into the chamber through their respective evaporation loops. These precursor vapor flows were mixed together with 100 sccm of hydrogen at a temperature of 180 - 200 ^{o}C and a pressure of 5 Torr.

2.2.4 DLE CVD Reactor Setup

Figure 2.6 shows the schematic diagram of the home-made syringe based DLE-CVD system. Common glass syringes do not have fittings that have tight seals; thus oxygen or water in the air can diffuse into the precursor solution through these leakage paths fairly easily. To overcome this problem, a stainless steel syringe (KD Scientific) with a 1/16” Swagelok fitting connection was used. The stainless steel syringe was controlled by an infusion/withdrawal syringe pump (KD Scientific, Model #KDS210). The syringe was positioned vertically in order to expel out any trapped gas bubble inside the syringe, which might cause inconsistent flow of the liquid solution. Two manual valves were added in order to avoid the air exposure to the 2-way ALD valve during bubbler refill.

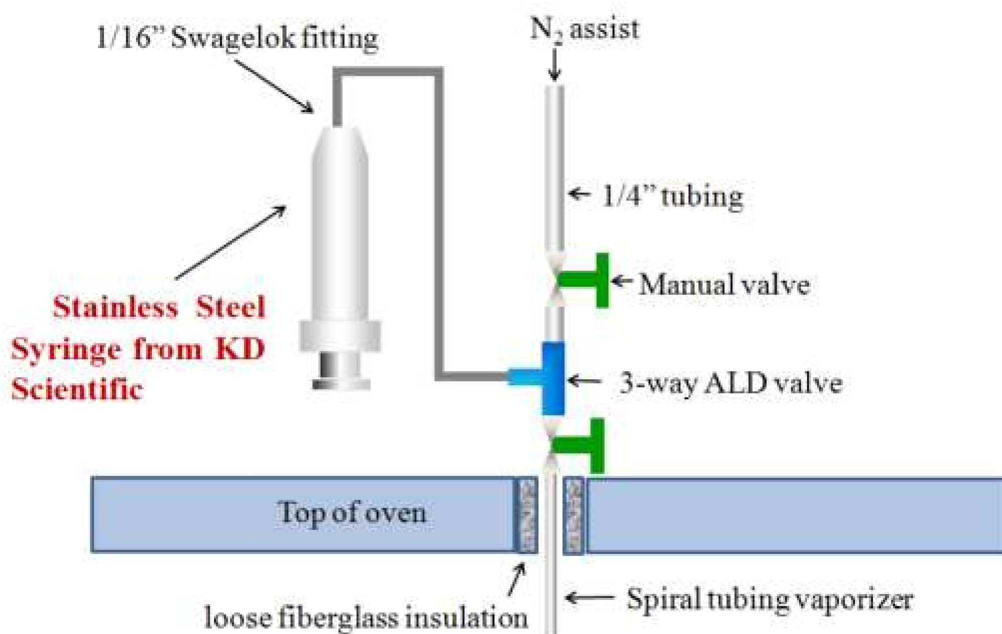


Figure 2.6. Schematic diagram of our DLE-CVD system.[37]

Figure.2.7 shows a schematic diagram of our DLE-CVD system for manganese based film deposition. The Mn precursor bubbler has a rounded glass viewport in the middle for performing visual checks on the current level of the precursor solution. The top of the bubbler is under a high pressure N_2 ambient, which serves as the driving force for the liquid flow. The flow rate of the liquid solution is controlled by a liquid mass flow controller (Brooks Instrument), which ranges from 0.05 to 1 sccm. The small amount of liquid delivered is assisted with 60 sccm N_2 gas flow to enter into the oven, which is kept at 150 ^{o}C. Lower temperatures could cause incomplete vaporization of the liquid droplets and hereafter the clogging of the flow path. After the liquid enters the oven, it travels through a long (3-4 meters) spiral tubing, which serves as a robust and reliable, low-cost thermal vaporizer for the complete vaporization of the liquid. The vapors of the metal precursors mix with the co-reactant gases right before

entering the reaction chamber. The reaction chamber was kept at 160 to 200°C during the deposition. Another bubbler filled with toluene is connected in parallel with the Ni precursor bubbler for the clean-up of the flow paths before their exposure to the air during the process of refilling the precursor. The liquid mass flow controller used in the system is relatively expensive. The inner flow path of the liquid MFC is very delicate; small particles, either from the ambient or formed by the trapped precursor due to the air exposure during precursor refill could readily clog up the inner flow paths.

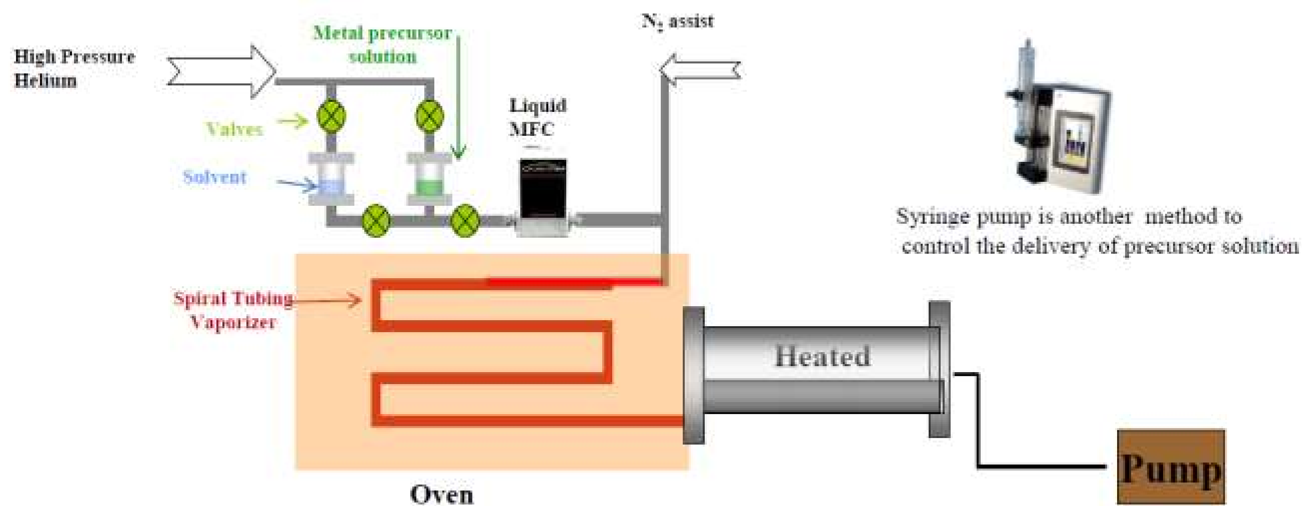


Figure 2.7. Schematic diagram of the reactant flow paths in a DLE-CVD system.

2.2.5 Characterization Methods

The sheet resistance of the as-deposited films on silicon oxide was measured by a four point probe station (Veeco Instruments; Model FPP-5000). The physical thickness of the film was measured by Field Emission Scanning Electron Microscope (FESEM; Zeiss FESEM Ultra Plus). The relative amount of metal deposited was measured by the X-ray fluorescence (XRF). The

crystalline phases were evaluated by transmission electron microscopy (TEM; JEOL 2100 TEM system). Depth profiling using X-ray photoelectron spectroscopy (XPS; ESCA Model SSX-110) was used to study the elemental composition. The surface roughness of the films was evaluated by atomic force microscopy (AFM; Asylum MFP-3D AFM system).

2.3 Results and Discussion

2.3.1 DLE CVD Process of Nickel Nitride thin films and conversion to Nickel Silicide

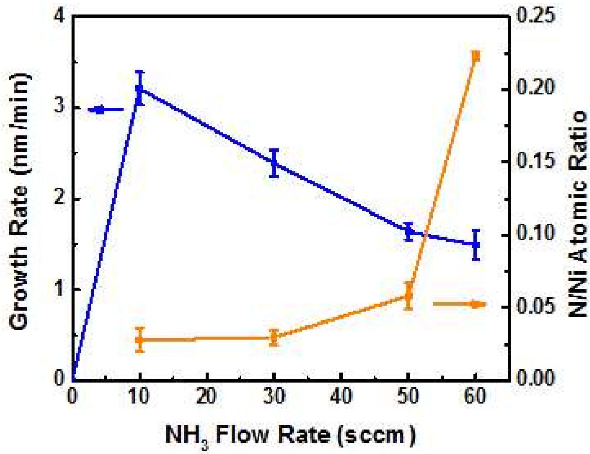
As mentioned previously, thermal ALD of NiN_x using $Ni(ipr\text{-}AMD)_2$ and H_2 or NH_3 as a co-reactant was reported by several groups. However, the growth temperature is relatively high (above 250 ^oC), and the growth rate is slow (< 0.5 A/cycle). In this Chapter, we discuss about the low temperature deposition of DLE-CVD of nickel nitride and nickel metal at substrate temperatures of as low as 160 ^oC with NH_3 and H_2. Nickel film can be converted to nickel silicide film at 470 ^oC.

When using NH_3 as the only co-reactant, the films contain substantial amounts of nitrogen. The XPS depth-profile in Figure 2.8 showed significant N (~20%) in the nickel nitride films.

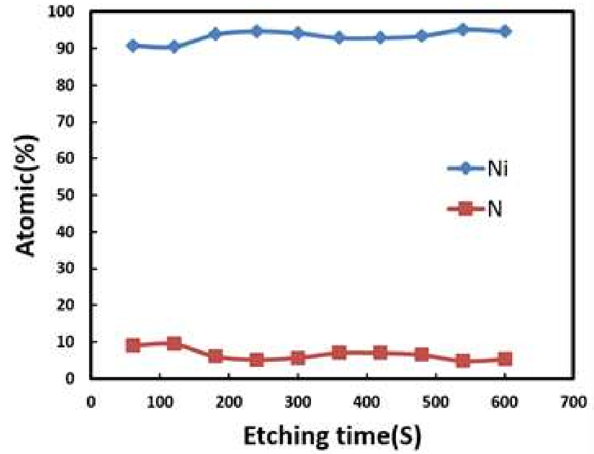
When using H_2 as the only co-reactant for the DLE-CVD nickel deposition, the growth rate is very slow at 200 ^oC or lower.

When H_2 is used as a co-reactant along with NH_3 in the process, significantly less carbon and nitrogen is incorporated in the film. For the films deposited using both NH_3 and H_2, XPS depth profile studies revealed less than 2% of C and O impurities inside the film regardless of the feed ratio of the two co-reactants. Furthermore, N content is lowered to less than 5%.

When NH_3 is used in addition to H_2 in the process, it significantly promotes the growth of nickel metal at the low temperature of 160 ^{o}C. Shimogaki and Gordon calculated the activation energy of different reactive pathways using the nickel amidinate precursor with and without NH_3, and found that NH_3 was effective at speeding up the deposition rate.[40] Our experiments also agreed with this result. With 10 sccm of NH_3 and 50 sccm of H_2 the growth rate at 160 ^{o}C reached 3 nm/min. In contrast, no film is deposited when no NH_3 is used. This suggests that the NH_3 adsorbed on the substrate surface encouraged the chemisorption of the cobalt amidinate precursor by reaction with the NH bonds on the surface. As shown in the Fig 2.9, the deposition rate decreases as the fraction of NH_3 increases in the reactant gas composition. Also the C and O impurities are undetectable in the XPS depth profile when NH_3 and H_2 are 10 sccm and 50 sccm in the reactant gas. These conditions are the optimized conditions that we use in the nickel nitride deposition.



(a)



(b)

Figure 2.9 (a) Growth rate and N/Ni atomic ratio plotted versus the NH_3 flow rate used during DLE-CVD process (keeping NH_3 + H_2 total flow rate as 60 sccm); (b) XPS depth profile of the Ni film deposited by optimized conditions (10 sccm NH_3 and 50 sccm H_2 as co-reactant).

The 5% N can be further reduced by annealing the as-deposited nickel nitride with 10 sccm NH_3 and 50 sccm H_2 in H_2 atmosphere at 160 ^{o}C without air-break after the DLE-CVD process. According to the N1s XPS spectra of the sputtered nickel nitride films (500 eV Ar+ sputtering for 480s to remove surface contaminations), the N content of Ni film is further reduced to below 0.9 at.%. To investigate the morphology of the Ni film, cross-section SEM and surface AFM images are presented in Fig.2.10, showing a thickness of 61.5 nm (20 mins deposition time) and a RMS value of 3.5nm.

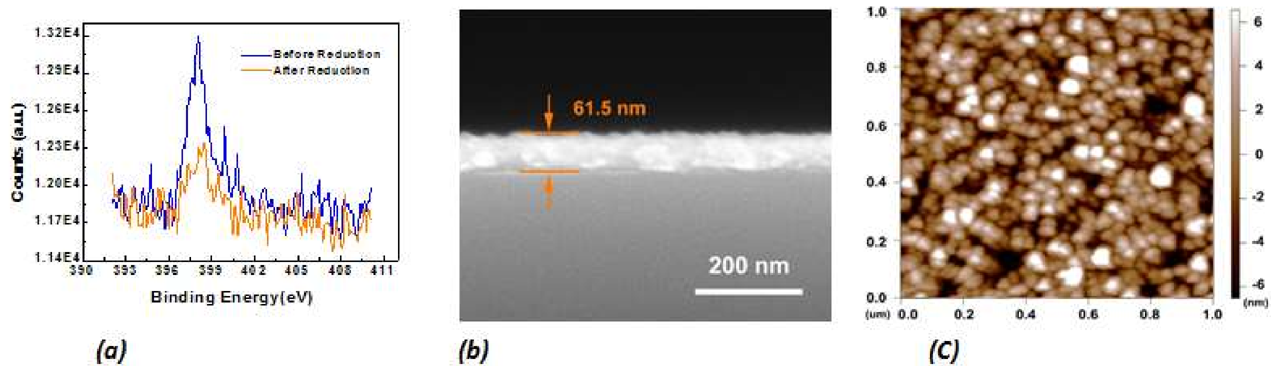


Figure 2.10. (a) N1s XPS spectrum of samples before and after reduction under H_2, showing anitrogen content drop;(b)The cross section SEM image of DLE-CVD Ni film;(c) Taping-mode AFM image on the surface of Ni film.

A ~40 nm thick nickel film inside a trench with aspect ratio of > 50:1 is shown in Figure 2.11. The thickness of the film at the bottom of the hole is equal to that on the top and the middle, confirming the good step coverage of DLE-CVD Nickle CVD process at 160 C with NH_3 10 sccm and H_2 50 sccm.

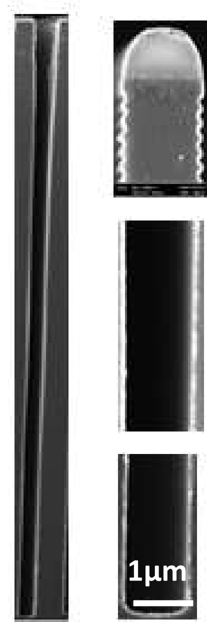


Figure 2.11. Cross-section SEM images of the Ni-coated trench sample.

The Ni-coated trench sample was annealed in N_2 at 470 ^{o}C for 3 min, during which Ni silicide was formed at the interface between Ni and Si. The cross-section SEM of the same region shown in Fig. 2.12. Based on the image, approximately 93 nm Ni silicide is formed at the interface and about 32 nm of Ni residue is left on top of Ni Silicide.

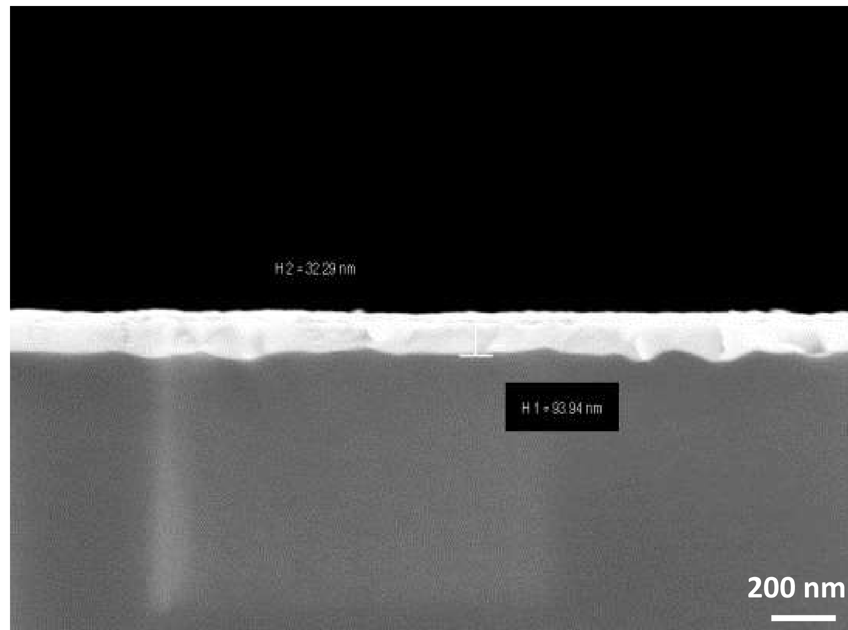


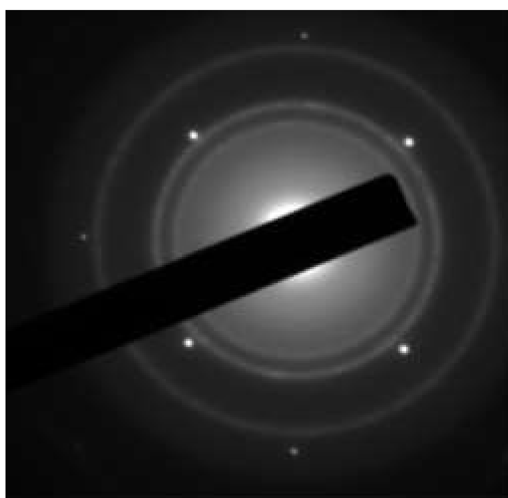
Figure 2.12. Cross-section SEM images of the nickel silicide sample.

2.3.2 DLE CVD Process of manganese Nitride and copper Thin films

Manganese Nitride

In this chapter, by DLE-CVD method, smooth and low resistance manganese nitride with excellent conformality in a very wide range of temperature window from 130 ^{o}C to 300 ^{o}C.

To deposit manganese nitride, ammonia was used as the only co-reactant gas, flowing at 60 sccm, combined with 5 g/h of precursor solution and 60 sccm of N_2 carrier gas. TEM and XRD measurements determined that the as-deposited manganese Nitride is in the phase of Mn_3N_2 as shown in Fig 2.13. The TEM sample is MnN_x film as deposited on the SiN_x TEM grid with DLE-CVD process at 160 ^{o}C. The diffraction rings correspond to hexagonal Mn_3N_2 (103), (110), (200). The XPS depth-profile in Fig 2.13 also showed significant N content (~35 at%) in the manganese nitride film. In addition, C was not detected by XPS inside the film since the film has less than about 1% of C which is under the detection limit of the XPS system. O was detected by XPS inside the film to be around 1.5% at.% of the film, this is probably a result of O having diffused into the film during the sample transfer from the reactor to the XPS chamber.



d (A)	Mn_3N_2 (d)	Index
2.43	2.40	103
2.12	2.10	110
1.47	1.48	200

Figure 2.13. TEM diffraction pattern on Mn_3N_2 (left) and their corresponding lattice spacing values calculated and compared to literature values (right).

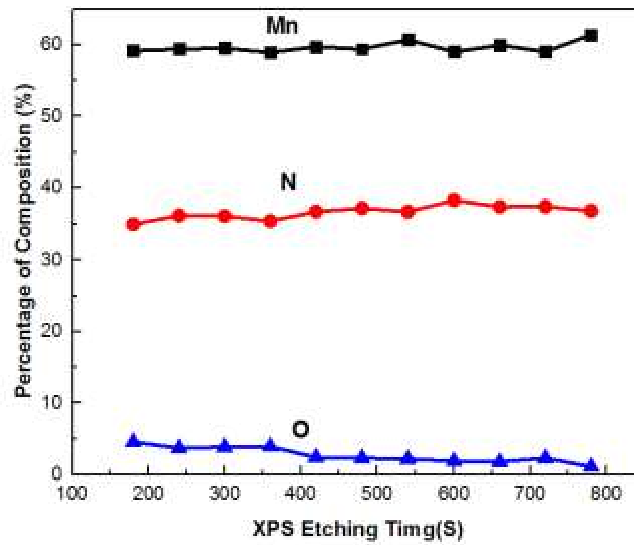


Figure 2.14. Elemental composition of the Mn_3N_2 film recorded during the XPS depth profile measurement.

The surface morphology of a manganese nitride film was examined using the AFM and found to be smooth with a roughness of approximately 8%.

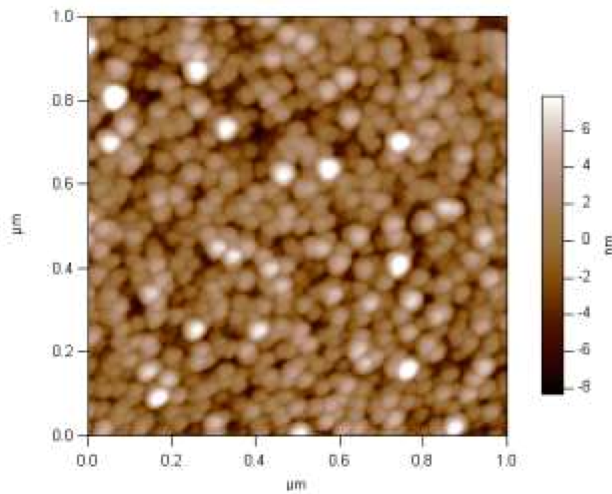


Fig2.15. Tapping-mode AFM image on the surface of Ni film

The step coverage of DLE-CVD MnN_x for different growth conditions was examined by depositing MnN_x on a silicon substrate containing holes with high aspect ratios. Then the coated substrate was hand cleaved to study the cross-section of the holes. The cross sectional SEM images in Fig. 2.16 shows MnN_x film deposited conformally inside a hole with aspect ratio of 48:1 (170 nm diameter and 8 um depth) obtained from Tokyo Electronics. The MnN_x film at the top, side wall and bottom of the feature are almost the same, showing nearly 100% step coverage.

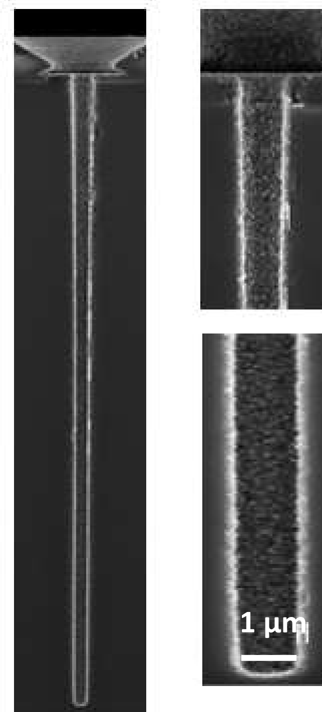


Figure 2.16. Cross-section SEM images of manganese nitride inside a hole

Growth Rate

The delivery rate of manganese precursor solution and temperature are the two most important factors that determine the growth rate of MnN_x.

Impact of the delivery rate

The delivery rate of the manganese precursor solution was varied to investigate whether the deposition rate has achieved saturation. MnN_x films were deposited at 160 ^{o}C with the conditions of 60 sccm of NH_3, maintained at 5 torr on a thermal oxide substrate for 20 minutes. The manganese precursor solution was delivered at rates from 2.5 g/hr to 20 g/hr. Figure 2.16 shows the deposition rate of DLE-CVD as a function of cobalt precursor solution delivery rate. The deposition rate is almost saturated at the precursor solution delivery rate of 10g/hr. Increasing the mangnese precursor delivery did not result to higher MnN_x growth rates.

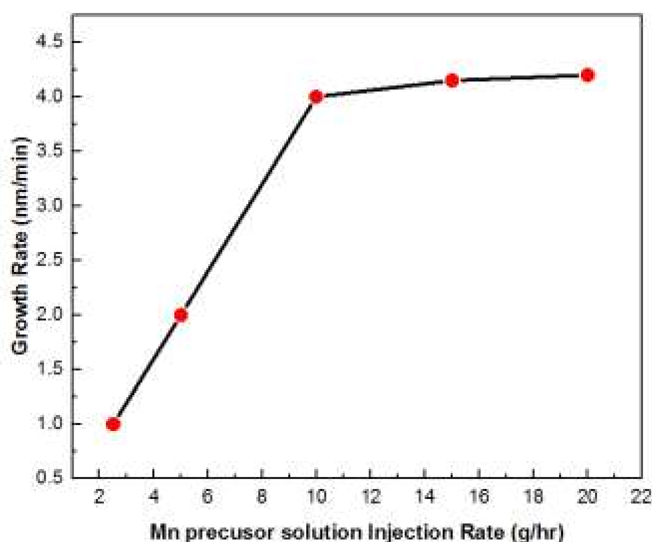


Figure 2.17. Delivery rate of manganese precursor solution and the resulting growth rate of MnN_x.

Temperature-dependence of Growth Rate

Manganese Nitride film deposition

MnNx films were deposited at various temperatures of 100 °C, 130 °C, 160, 180 °C, 200 °C with NH_3 flow rate at 60 ccm, at 5 torr with the Mn precursor solution injection rate of 5 g/hr on thermal oxide substrates. The growth rate increases as the deposition temperature rises.

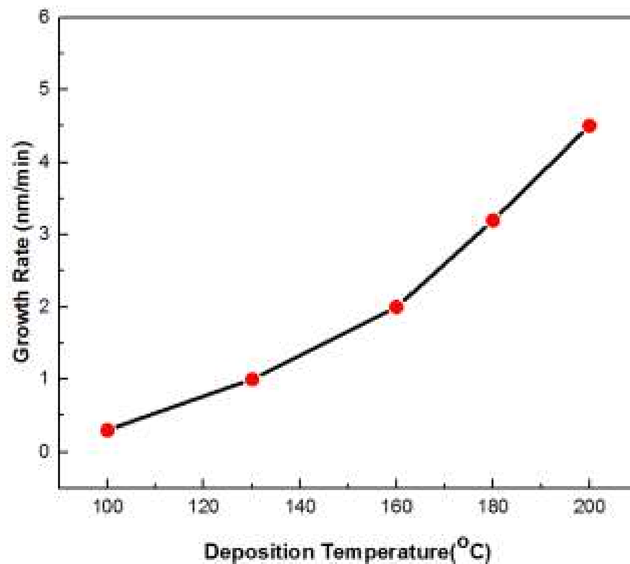


Figure 2.18. Substrate temperature of manganese precursor and the resulting growth rate of MnN_x.

Copper film deposition

In this chapter, continuous and highly conformal copper-manganese films are deposited by DLE-CVD process. The vapor delivery rate from the DLE system is stable, reproducible and accurately known because the concentration of the solution and the liquid and carrier gas injection rates are known. Smooth and continuous copper films can be deposited within a temperature

window of 180 °C to 200 °C. The DLE system for copper deposition used the syringe based DLE-CVD system.

To deposit copper, H_2 is used as the only reactant gas for copper DLE-CVD deposition, flowing at 100 sccm. Combined with 0.1 ml/min of precursor solution and 60 sccm of N_2 carrier gas, the molar percentages and partial pressures of the gas mixture introduced into the reactor were 0.2% or 0.02 Torr Cu precursor vapor, 2.8% or 0.28 Torr trihexylamine, 65% or 3.25 Torr H_2 and 32% or 1.6 Torr N_2.

The resistivity of copper film deposited by DLE-CVD system was 3 μohm.cm. The surface morphology of copper was examined by AFM. The copper thin film deposited by the DLE-CVD process on the manganese nitride underlayer is fairly smooth with a root-mean-square roughness equal to 6.2% of its thickness.

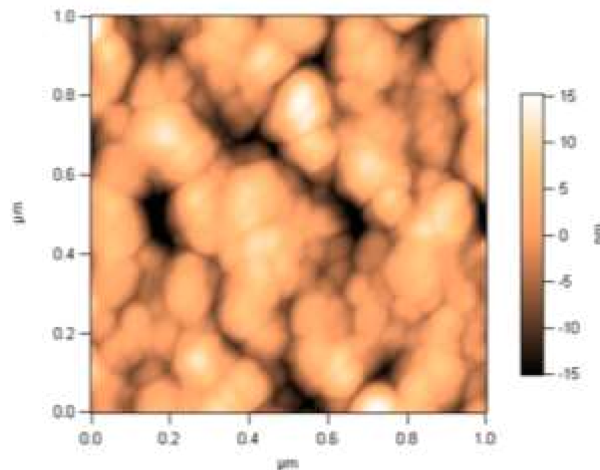


Figure 2.19. 2D AFM map of Cu metal showing the very smooth films produced by the DLE-CVD Cu process.[41](collaborative work with Dr. Yeung Au)

The step coverage of DLE-CVD copper for different growth conditions was examined by depositing copper on a silicon substrate with high aspect ratio trenches having MnN_x film previously deposited on it.

Then the coated substrate was hand cleaved to study the cross-section of the trenches. The cross sectional SEM images in Fig 2.18 show copper films deposited conformably inside a trench with an aspect ratio of 25:1 (0.5 um diameter and 12.5 um depth). The copper film at the top, side wall and bottom of the feature are almost the same, showing nearly 100% step coverage.

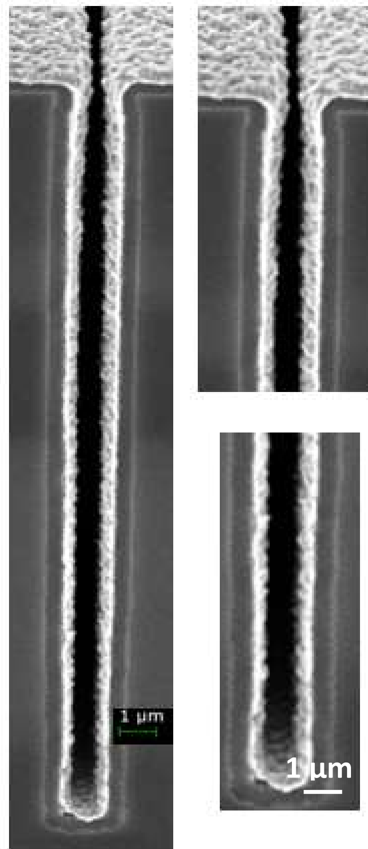


Figure 2.20. Cross-section SEM images of the Copper Trench sample

Growth Rate

The delivery rate of copper precursor solution and temperature are the two most important factors to determine the growth rate of copper film.

Impact of the delivery rate

The delivery rate of copper precursor solution has been varied to investigate whether the deposition rate has achieved saturation. copper films were deposited at 200 ^{o}C with the conditions of 100 sccm of H_2, maintained at 5 torr on thermal oxide with MnN_x film for 15 minutes. The copper precursor solution was delivered at rates from 0.02 ml/min to 0.15 ml/min. Figure showed the deposition rate of DLE-CVD as a function of copper precursor solution delivery rate. The deposition rate is almost saturated at the precursor solution delivery rate of 0.05 ml/min. The increased copper precursor delivery rate did not result in higher copper growth rates.

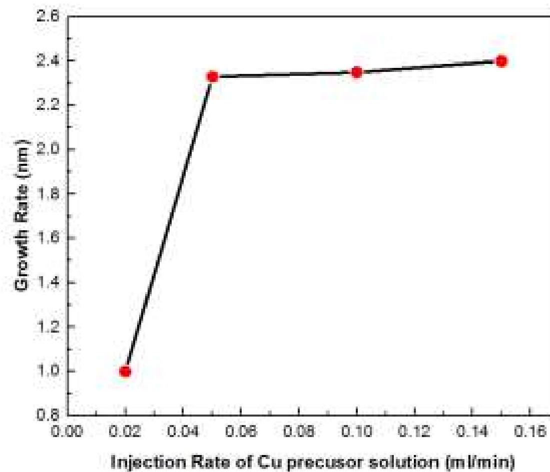


Figure 2.21. Substrate temperature and injection rate of copper precursor solution, and the resulting growth rate.

Temperature-dependence of Growth Rate

Copper film

Copper films were deposited at various temperatures of 180 °C, 190 °C, 200 °C with 100 sccm of H_2, maintained at 5 torr on thermal oxide with the Cu precursor solution injection rate as 0.05 ml/min. The growth rate increases as the deposition temperature rises. However, when the deposition temperature goes up higher than 200 °C, copper agglomeration appears due to the high surface diffusion rate.

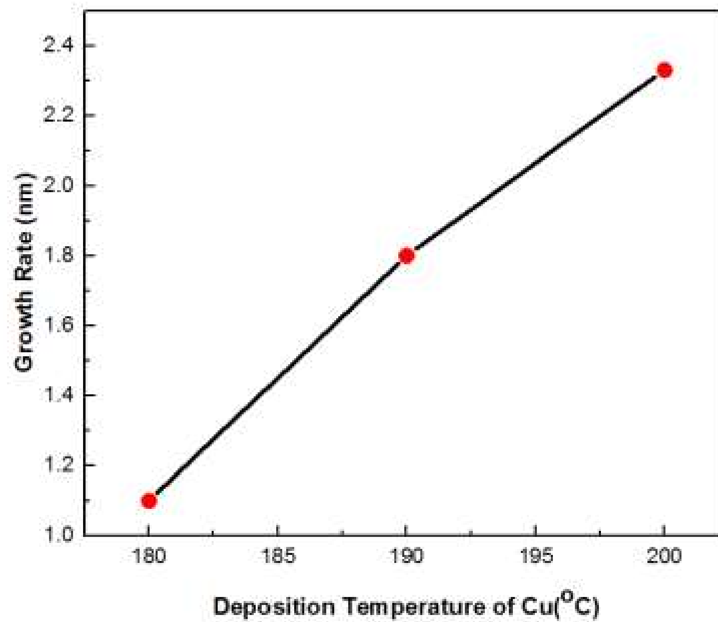


Figure 2.22. Substrate temperature of copper precursor and the resulting growth rate of Cu.

2.4 Conclusions

DLE-CVD processes employing $Ni(MeC(N^tBu)_2)_2$ with NH_3 or a mixture of NH_3/H_2 gases as the co-reactant produced smooth and continuous NiN_x and Ni films with excellent step coverage in holes with aspect

ratios over 50:1; the growth rate of NiN_x film with the DLE-CVD process is much higher than the rate achieved with ALD or bubbler-based CVD processes. The growth rate of DLE-CVD films was increased and the nitrogen content of the Ni films reduced by using NH_3/H_2 mixture as the reactant gas. Nickel silicide formed from Ni film on silicon by annealing at 470 ^{o}C for 3 mins .

DLE-CVD processes employing bis(*N,N′*-di-*tert*-butylacetamidinato)manganese(II) with NH_3 or a mixture of NH_3/H_2 gases as the co-reactant produced smooth and continuous MnN_x films with excellent step coverage in holes with aspect ratios over 50:1, the growth rate of MnN_x film with DLE-CVD process is much higher than ALD and bubbler based CVD processes.

DLE-CVD processes employing copper(*N,N′*-di-*sec*-butylacetamidinate) dimer with H_2 gas as the co-reactant produced smooth and continuous Cu films with excellent step coverage in holes with aspect ratios over 25:1; the growth rate of Cu film with DLE-CVD process is much higher than ALD and bubbler based CVD processes. The growth rate of DLE-CVD films was increased as a result of the higher vapor concentration in the DLE-CVD process.

The DLE-CVD process of nickel-based, manganese-based and copper-film enhanced the delivery of precursor vapors, not only enhance the growth rate but also the step coverage in high-aspect ratio structures.

Reference

[32] J. Yang, K. Li, J. Feng, and R. G. Gordon, "Direct-liquid-evaporation chemical vapor deposition of smooth, highly conformal cobalt and cobalt nitride thin films," *J. Mater. Chem. C*, vol. 3, no. 46, pp. 12098–12106, 2015.

[33] K. P. S. Three-dimensional, A. Ibm, and A. Ibm, "Three- dimensional silicon integration," *Int. Bus.*, vol. 52, no. 6, pp. 553–569, 2008.

[34] G. B. Raupp and T. S. Cale, "Step coverage prediction in low-pressure chemical vapor deposition," *Chem. Mater.*, vol. 1, no. 2, pp. 207–214, 1989.

[35] Z. Li, S. T. Barry, and R. G. Gordon, "Synthesis and characterization of copper(I) amidinates as precursors for atomic layer deposition (ALD) of copper metal," *Inorg. Chem.*, vol. 44, no. 6, pp. 1728–1735, 2005.

[36] G. G. New, N. Amidinate, A. L. D. Cvd, and C. Link, "New Ni Amidinate Source for ALD / CVD of NiNx , NiO and Ni The Harvard community has made this article openly available . Please share how this access benefits you . Your story matters . Citation Accessed," 2015.

[37] Z. Li, "Atomic Layer Deposition and Direct-Liquid-Injection Chemical Vapor Deposition of Nickel Nitride Films and Their Conversion to Nickel Silicide Films," 2011.

[38] A. Kafizas, C. J. Carmalt, and I. P. Parkin, "CVD and precursor chemistry of transition metal nitrides," *Coord. Chem. Rev.*, vol. 257, no. 13–14, pp. 2073–2119, 2013.

[39] R. G. Gordon, S. Barry, R. N. R. Broomhall-dillard, V. A. Wagner, and Y. Wang, "VOLATILE LIQUID PRECURSORS FOR THE CHEMICAL VAPOR DEPOSITION (CVD) OF THIN FILMS CONTAINING TUNGSTEN Roy G. Gordon, Seán Barry, Randy N. R. Broomhall-Dillard, Valerie A. Wagner and Ying Wang Department of Chemistry and Chemical Biology, Harvard University," *Mat. Res. Soc. Symp. Proc.*, vol. 612, no. Cvd, pp. D9.12.1–D9.12.6, 2000.

[40] S. Ravasio, T. Momose, K. Fujii, Y. Shimogaki, M. Sugiyama, and C. Cavallotti, "Analysis of the gas phase kinetics active during GaN deposition from NH<inf>3</inf> and Ga(CH<inf>3</inf>)<inf>3</inf>," *J. Phys. Chem. A*, vol. 119, no. 28, pp. 7858–7871, 2015.

[41] Y. Au, "Chemical Vapor Deposition of Thin Film Materials for Copper Interconnects in Microelectronics," 2012.

Chapter 3 DLE CVD Nickel-based thin film for local interconnects in 3D microprocessors and Atom Probe Investigation

3.1 Introduction

Metal silicides reduce the resistivities of both gate and source-drain contacts in MOSFET structures. Metal silicides can create contacts to silicon that demonstrates smaller resistivity and lower contact resistance, good thermal stability and high compatibility with the semiconductor manufacturing process. Ni, Co and Ti are usually considered favorable contact metals to silicon because they can all form stable low-resistance silicides at their interfaces with silicon at elevated temperatures.[42] In advanced semiconductor manufacturing processes, the formation of Ni silicide is currently the preferred method for improving the contact with silicon due to its more moderate formation temperature, higher conductivity and smoother interface than those that Co and Ti silicides can provide. [43]

The greatest challenge for Ni silicide is to reduce the silicon consumption during the silicide formation while maintaining low resistivities, low formation temperature and high stability. Ni monosilicide phase is introduced instead of $NiSi_2$ or Ni_2Si. These requirements can be met since NiSi has a low resistivity of around 14 $m\Omega$-cm and only requires formation temperatures below 400 ^{o}C. In contrast, $NiSi_2$ requires over 600 ^{o}C and Ni_2Si is unstable when interfacing with silicon.

[44] Therefore, to enable higher-performance silicon devices, processes for forming high-quality NiSi at Ni/Si interfaces are needed.

In modern ultra-large-scale integrated (ULSI) architectures, blocks with different functionalities are connected three-dimensionally, making it necessary for both semiconductor devices and interconnects to fabricated in structures with high aspect ratios.[45][46] Fin-type field-effect transistors (FIN-FET) are a type of three dimensional transistors in the ULSI process, which use a conducting channel that rises above the level of the insulator, creating a thin silicon structure and shaped like a fin.

As Moore's law is extended, the aspect ratios of fins become higher and higher. The high-aspect ratio silicon fins require conformal coating of dielectrics, amorphous silicon gates, as well as the metal/silicide contacting with a-Si gate, as illustrated in Figure.3.1 (a). Also, in multi-layer electronics, connections may require the formation of conformal Ni on copper lead wires as shown in Figure 3.1(b).

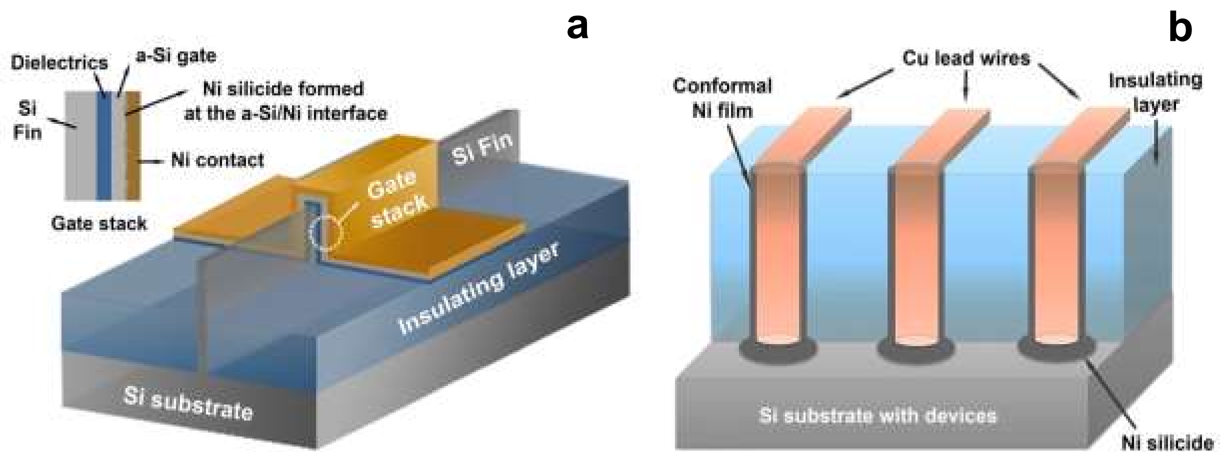


Figure 3.1. (a) Illustration showing the various layers that needs to be coated over the Si fin. (b) Cross section diagram depicting highly conformal Ni films overlaying Cu lead wires.

Great difficulties have been encountered by the industry in the deposition of conformal and uniform metal films inside high-aspect-ratio structures due to the anisotropic nature of most physical vapor deposition techniques currently available. [5] As indicated in Chapter 2, DLE-CVD of Ni metal on Si, which can be readily transformed into NiSi at its interface with silicon, has been introduced in recent research reports. [47][13] DLE-CVD provides highly conformal coatings of Ni thin films and thus conformal NiSi layers; however the reported compositional and structural characterizations of these materials have been mostly conducted on planar samples rather than directly on the specimens deep inside high-aspect-ratio structures. Due to the morphological and surface differences, the properties of the material inside the high-aspect-ratio structure may differ from the material in the planar surface. In this sense, the composition analysis of those materials deep inside of high-aspect-ratio structures is critical for the FIN-FET devices. Atom Probe Tomography (APT) is a high-precision characterization method with atomic resolution from both compositional and morphological points of view. With focused ion beam (FIB) sample preparation techniques, specimens from deep inside of high-aspect-ratio structures can be physically lifted-out and sharpened into ultrasmall needles (~30 nm tip diameter) suitable for APT analysis. [48]

In this chapter, APT analysis is used to show how high-purity NiSi has been successfully formed from DLE-CVD Ni films inside trench structures. Ni and Si distribution in the specimens from both outside and inside of the high aspect ratio trench have been observed to be highly

uniform, with a 1:1 Ni to Si atomic ratio, while all impurities only present at ~0.1 atomic percent.

3.2 **Experiments**

The high-aspect-ratio trench samples (10:1 aspect ratio, Figure 3.2 (a)) test structures were fabricated by Bosch-type deep silicon reactive ion etching (DRIE) process with SF_6 and C_4F_6 gases. In the fabrication process, 1 μm of ZEP-A e-beam resist patterned by e-beam lithography was used as the soft mask.

The chemical vapor deposition of NiN_x was conducted with the home-made direct liquid evaporation (DLE) system which has been discussed in Chapter 2. $Ni(MeC(NtBu)_2)_2$ precursor solution (20% w.t.% in tetradecane) was injected by a syringe pump at a rate of 0.1 mL/min into the heated vaporization loop inside an oven that was heated to 150 ^{o}C. During the vaporization, the precursor vapor was mixed with 60 cubic centimeters per minute (sccm) purified nitrogen and then introduced into a reactor chamber preheated to 160 ^{o}C. As a co-reactant, 10 sccm ammonia premixed with 50 sccm H_2, 60 sccm purging gas (N_2) was also introduced into the reactor chamber. Using a pressure controller, the total pressure in the reactor was regulated at 10 Torr, which was then maintained throughout the deposition process. Inside the reaction chamber, an aluminum half-cylinder was used as the sample holder, in which a resistive heater and a thermocouple were embedded to slightly elevate the holder temperature to about 10 ^{o}C

above the chamber wall. In order to obtain Ni silicide, the as deposited NiN_x film on Si substrate was first reduced to Ni, and then annealed to form Ni silicide at the Si-Ni interface. The reduction was performed under H_2 atmosphere for 0.5-1.0 h at 200 ^{o}C, and the annealing was at 470 ^{o}C for 3 min.

Laser-mode APT analysis was used to analyze both NiN_x and NiSi thin film. The analysis conditions of NiN_x thin film were optimized for pre-sharpened micro (PSM) tips APT specimens. PSM tips are an ordered collection of tall (~100 μm) Si posts formed on Si coupon by standard microelectromechanical systems (MEMS) techniques. The Si PSM tips (30-50 nm) were coated by ~30 nm DLE-CVD NiN_x thin film, which made the PSM tips into APT specimens with diameter around 100 nm. The APT specimens were cut with a dual-beam focused ion beam (FIB) system. Specimens were collected from both outside and inside of the trench by FIB lift-out technique along a direction parallel to the sample surface, followed by annular milling with Ga^+ ion beam to sharpen the specimens into needles with radius between 20 nm and 50 nm and with shank angles around 10°. The analyses were carried out at 50k under a vacuum pressure lower than $5x10^{-11}$ torr. Pulsed 532 nm laser light was applied to assist ion evaporation, of which the pulse energy was set to be 50 pJ and the pulse frequency set to be 100 kHz. The average evaporation rate was maintained at 0.5 ion per pulse. Data reconstruction was performed with IVAS software incorporating standard reconstruction algorithms, enabling the extraction of three-dimensional quantitative compositional and structural information.

The cross-section morphology of the thin films was analyzed using the Zeiss Ultra55 field-emission scanning electron microscope (FE-SEM), from which the thickness of each film is measured. X-ray photoelectron spectroscopy (XPS) was used to perform depth-profile elemental. The surface roughness of the films was analyzed by atomic force microscopy (AFM). The Cameca LEAP 4000X HR system was used for APT analysis in this report.

3.3 Results and Discussion

3.3.1 DLE CVD of Nickel Nitride and Nickel Metal in high aspect ratio nanostructures

Silicon trenches with aspect ratios of 10:1 provide a vehicle to show the conformality of DLE-CVD of NiN_x and its conversion to Ni silicide. These high aspect ratio features were fabricated into silicon trenches via the Bosch-type DRIE process. Fig 3.2 shows a cross-sectional SEM of the resulting trench, of which width and depth are 700 nm and 7.00 μm, respectively. After 90 minutes of Ni DLE-CVD and 30 minutes of H_2 baking, we formed a highly conformal Ni coating in the trench. The Ni DLE-CVD process is able to coat the test structure with extremely high uniformity and conformality through the entire DLE-CVD deposition process, measuring a film thickness of 262 nm both inside and outside of the trench. Of note, the aspect ratio of trenches increases up to 40:1 when the deposition approaches the end, since the Ni coating reduces the width without reducing the depth of the trench significantly.

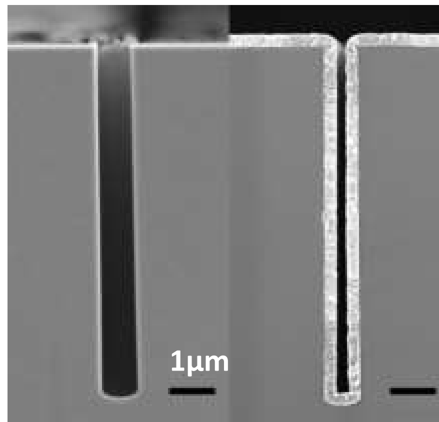


Figure 3.2 Cross-section SEM images of silicon trenches before (a) and after (b) Ni deposition to demonstrate the conformality of the deposited film

3.3.2 Conversion to Nickel Silicide

The Ni-coated trench sample was annealed in N_2 at 470 ^oC for 3 min, during which Ni silicide is formed at the interface between the Ni and Si. The cross-sectional SEM of the same region shown in Fig. 3.2 is presented in Fig 3.3. Based on the image, approximately 160 nm Ni silicide formed at the interface and about 100 nm of Ni residue is left on top of Ni Silicide.

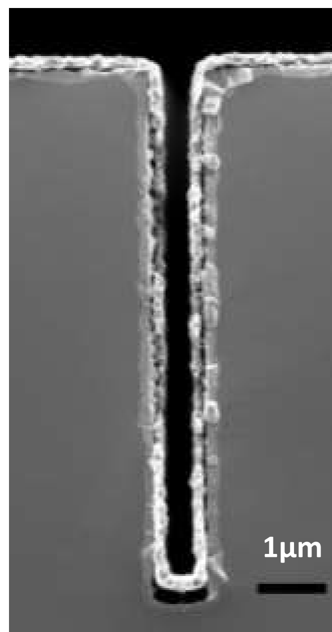


Figure 3.3 Cross-section SEM images of silicon trenches after Ni Silicide was formed.

3.4 Specimen Preparation for Atom Probe Tomography

As with many experimental techniques, specimen preparation for atom probe tomography is quite crucial for successful results. To achieve the field strengths required for field evaporation in atom probe, the feature of interest must be positioned near the apex of a sharp needle-shaped tip. The specimen preparation is the essential and most challenging part of the experiment.

3.4.1 Specimen Geometry Requirements

The key geometry requirements of an atom probe specimen are as follows:[29]

1. A sharp needle-shaped specimen is needed with the specimen apex radius between 50 and 150 nm and the semi-angle (also named as the half shank angle) less than 10°. The sharp tip is required to generate an intense field for field evaporation.
2. A smooth surface with no protrusions, grooves or cracks.
3. A circular cross section. The data reconstruction is based on the assumption of a hemispherical cap; any deviation from this shape such as surface protrusions, or asymmetrical cross section, will cause artifacts in the reconstructed data.
4. The feature of interest must be positioned within approximately 100 nm of the specimen apex to ensure that it is included in the acquired datasets.
5. Sufficient specimen length and tip clearance to prevent shielding from the support structure and an absence of “secondary tips”, or sharp protrusions in the vicinity of the

tips. Any other sharp features on the sample should be at least ~100µm away from the tip. Otherwise, if those sharp features are sharp enough to emit ions by field evaporation simultaneously, it will interfere the data collection from the main specimen.

6. The specimen needs to be robust enough mechanically to allow for significant evaporation to occur. The fracture of a specimen will terminate the data collection and stop the experiment and sometimes may contaminate the local electrode.
7. The specimen must be self-supporting.
8. For voltage-pulsed atom probe, the electrical resistance to the apex must be about 10^2 ohm or less. For the typical geometry, the specimen resistance is dominated by the last 10 um or so. This requires a specimen resistivity less than ~ 0.05 ohm.cm assuming that the material is uniform.

The small and strong specimen enables the high electric field (~10 - 50 V nm^{-1}) necessary for field evaporation. The needle-shaped specimen is the primary optic of the microscope; specimen preparation forms a critical step in the success of APT analysis.

3.4.2 Deposition-Based Specimen Preparation

The needle shaped specimens are formed by electropolishing. Electropolishing has been the main method used to fabricate these needles from metal wires, whiskers, or blanks cuts (typically 0.25 ×0.25× 10 mm^3) from bulk materials. However, electro polishing cannot be directly applied to thin film materials ATP sample preparation.

Vapor deposition techniques are able to coat the surface of sharp needle. Therefore, instead of fabricating a needle shaped specimen from the thin film sample, thin films could be directly deposited on the surface of the sharp needle which can be ready for the ATP test.

Metal sharp needles can be prepared by electro polishing; however the quality of the commercial electropolished metal wires is not consistent. Evaluation of the initial shape of the metal wires is an important step before determining the thickness of thin film coating. Pre-sharpened microtips (PSMs) coupons are an ordered collection of Si posts (~100 μm) formed by microelectromechanical systems (MEMS) techniques. The local electrode atom probe enables the field evaporation exclusively from a single needle-shaped specimen located among a field of similar needle-shaped specimen. Figure 3.4 illustrated the images of PSMs before any coating and PSMs coated with thin film materials for test.

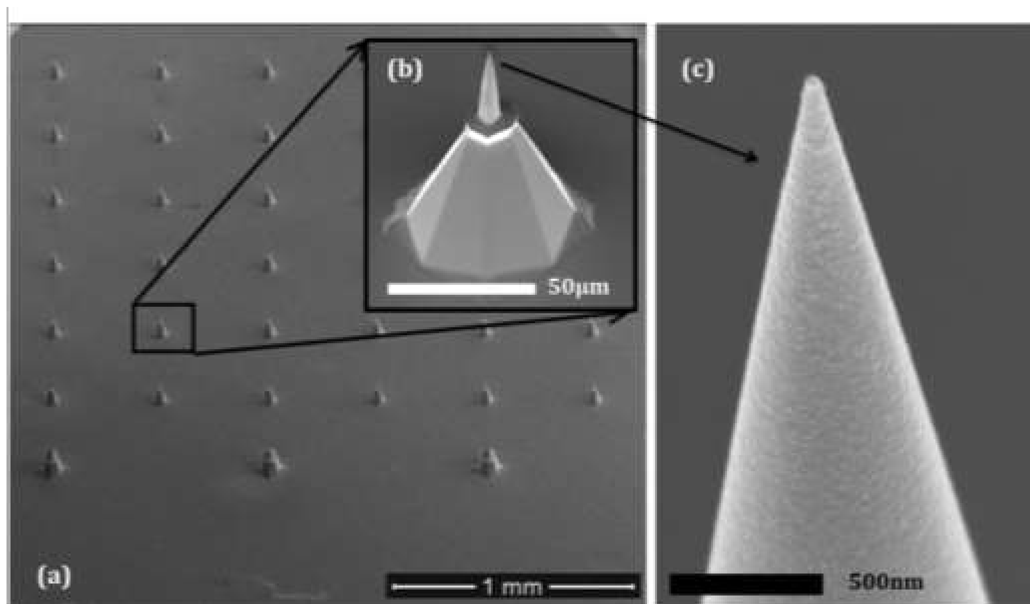


Figure 3.4. (a) An array of tips on a pre-sharpened microtip (PSM) coupon. (b) Close up image of the single PSM structure. (c) Highly magnified view of the tip of the PSM.[32]

The array of microtips in the PSM makes the ATP specimen preparation quite efficient. The thin films coated on the microtips are the features of interest, enabling APT analysis with a small requirement of material, parallel processing of large numbers, uniformity of shape and position, easy access to thin films on substrates, and low invasiveness on the specimen. These advantages are helpful in optimizing the APT analysis conditions of materials with complex structures.

Specimen preparation by directly depositing on the PSMs or on electropolished wires is an efficient and economical way to explore different experimental conditions for analyzing thin film materials for the first time. However, site-specific specimens cannot be investigated through this method.

In the investigation of nickel nitride thin films, PSM were utilized in the optimization of the APT analysis conditions. For specimens extracted from high-aspect ratio trench samples, Focused Ion Beam (FIB)-Based Specimen Preparation process was used, which will be discussed in the following part of this chapter.

3.4.3 Focused Ion Beam (FIB)-Based Specimen Preparation in ultra high aspect ratio nano structures

FIB-based specimen preparation methods offer the ability to fabricate atom probe specimen from a significantly wider range of materials and alternative specimen geometries than traditional methods. Specimens consisting of multilayer films, semiconductor devices, carbon

filaments and whiskers, ceramics are all can be prepared by the FIB process. The coupon extraction (lift-out) process has been used for site-specific specimen preparation for features such as boundaries, interphase interfaces, low volume fraction or inhomogeneously distributed phases, coarse precipitates, as well as ion-implanted and subsurface regions. Additionally, the FIB could be used as the final step to polish the specimen to correct artifacts and ensure a circular cross section with a smooth surface.

There are two stages in the FIB-based process. In the first stage, a post is extracted from the region of interest. The blank is mounted on a support post with a layer of Pt or W deposition. The post or the blank is then sharpened into the atom probe needle shaped specimen by an annular milling technique in which the outer and inner diameters of a circular mask and the milling current are decreased progressively. Figure 3.5

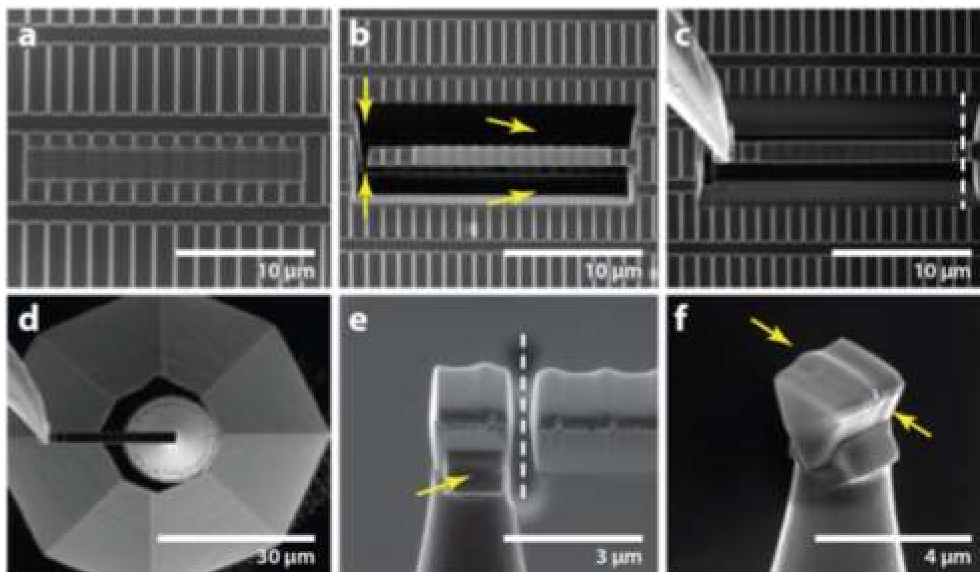


Figure 3.5. Illustrated and described the FIB-based site-specific specimen preparation in the FINFET case.[49]

The major concern of using the FIB-based technique is the damage dealt to the specimen by the ion beam. Commercial FIB uses gallium liquid-metal ion sources with accelerating voltages between 2 and 30 keV where gallium metal ions induce damage and artifacts in the specimen. In order to minimize the damage, a W layer is usually used to cap the region of interest.

The FIB-based method takes a long time (several hours to days) for sample preparation. It also has a steep learning curve for mastering its operation.

3.5 Atom Probe Tomography Investigation of Nickel Nitride Thin Films in Ultra high aspect ratio nano structures

Nickel nitride films were deposited by DLE-CVD method using bis(*N,N'*-di-*tert*-butylacetamidinato)nickel(II) precursor at 160 ^oC. DLE-CVD NiN_x with NH_3/H_2 as the reactant gas has demonstrated excellent conformality and controllable growth rate to coat the PSMs for ATP analysis. To investigate the NiNx film in the high aspect ratio nano structures, the FIB process was used to prepare ATP specimens.

3.5.1 Optimizing the ATP analytical conditions for Nickel Nitride Thin Films with PSM specimens

As discussed in the first chapter, ATP analysis has two main pulsing modes, HV (high voltage) pulsing and laser pulsing. HV-pulsing mode is limited to conductive materials, such as metals. Laser-pulsing is applicable to wide range of materials, both conductive and non-conductive materials. NiN_x is conductive, so both modes can be used for NiN_x coated PSMs.

The adjustable parameters in ATP experiments include the specimen temperature and the detection rate. The specimen temperature is typically held between 20 and 50 K to lower the surface diffusion rate. ATP experiments are generally conducted at a constant detection rate. The target detection rate is usually set to about a few atoms per 100 or 1000 pulses on average, or between 0.2% and 5% probability of an atom per pulse. The detection rate increases with the electrical field strength at the surface of specimen. An excessive electrical field may cause several issues in the ATP test. For example, specimens maintained at higher electric fields generate more ions per pulse, and thus are more likely to fracture. The probability of multiple events during one pulse increases with increasing detection rate. The relative amplitude of the background is generally lower at higher detection rates.

In the HV-pulsing mode, the adjustable parameters contain the pulse fraction and the pulse rate. The pulse fraction is defined as the ratio between the amplitude of the HV pulses and the DC standing voltage. The pulse fraction needs to be modified to avoid the preferential departure or retention of any given species at the surface of the specimen. Generally higher pulse rates are desirable for atom probe analysis. However, a higher pulse rate translates into a shorter time detection window, which might not be long enough to detect complex ions with longer flying time. Lower repetition rates must be used for compound materials which tend to exhibit field dissociation of large molecular ions.

Yield (# of ions collected)	DR (Detection Rate) (%)	Pulse Energy (PJ)	Pulse Frequency (Hz)	Multiple Event (%)	Background (PPm/nsec)	Fractured or Survived
2M	0.15	100	50K	4%	~10	survived
1.5M	0.2	100	100K	6%	10~12	survived
800K	0.25	100	100K	10%	~60	Fractured

Table 3.1. Summarized the atom probe investigations of NiNx coated PSMs using HV-pulsing mode. As discussed earlier, higher detection rate and high pulse rate might cause specimen fracture. The background noise level is relatively high for APT analysis.

In the laser-pulsing mode, the adjustable parameters include the laser wavelength, the size of the laser spot and its position along the specimen's shank, the laser energy, and the pulse frequency. The equipment supplier already preset most of these parameters. The CAMECA 3D atom probe (LEAP 4000XHR) at Harvard Center of Nanoscale System uses a 355 nm UV laser with 3μm (4σ) spot size. Finding the optimal position of the laser spot on the specimen is the most important and the most challenging part in operating the system. Successfully doing so guarantees the largest detection rate for a certain set of experimental conditions. The laser energy and the pulse frequency are normally adjusted to optimize the results further.

Preferential evaporation will change the ATP result significantly since it may cause the specific loss of the atoms with lower evaporation field. As a result, the pulse energy was adjusted to avoid preferential evaporation.

3.5.1.1 ATP analysis of Sample preparation on PSM

Around 30 nm thick NiN_x film was deposited on the PSM as shown in the SEM image below, with the final diameter of the top of the tip being around ~96nm which is the perfect thickness for ATP analysis.

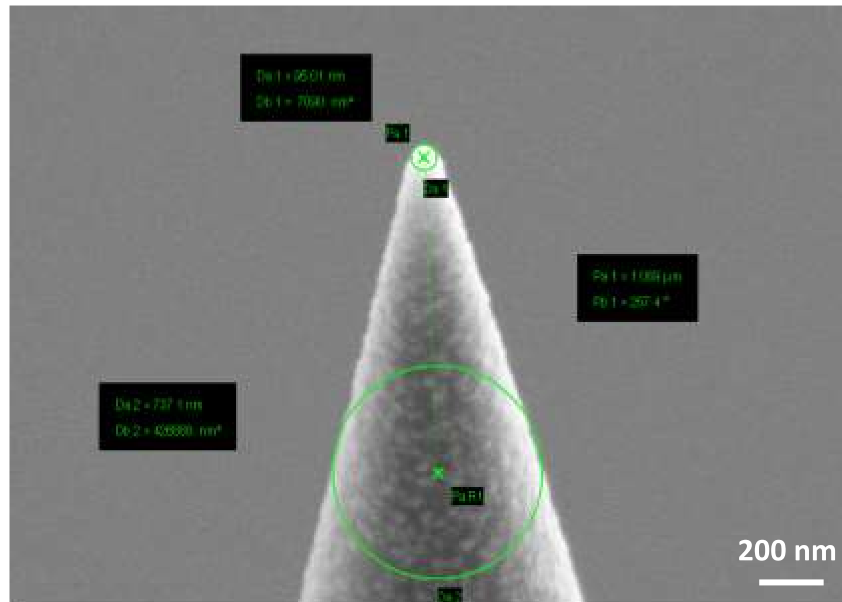


Figure 3.6. The NiNx PSM ATP sample

3.5.1.2 Mass Spectrum Analysis

To study the N distribution of in DLE-CVD NiN_x thin films on PSMs, the mass spectrum is complicated because of the underlying Si microtip. The mass to charge (m/n) ratio of Si overlaps with N. The m/n ratios of Si^{2+} and Si^{1+} are 14, 14.5, 15, 28, 29 and 30 Da. On the other hand, the m/n ratios of N^{1+} and N_2^{1+} are 14, 15, 28, 29 and 30 Da. The difference of m/n ratio for the N and Si are at 14.5 Da. It's quite challenging to distinguish the mass spectrum decomposition

between Si and N. The possible solution is through the compositional map. In the analysis, all the peaks in the position of m/n ratio as 14, 14.5, 15, 28, 29 and 30 Da can be assigned as Si atoms first. A region with very high concentration of Si atoms indicated the location of Si microtip region. Since only the very top part of NiN_x thin film materials is needed for the ATP analysis, the region of interest can be simply clipped by the IVAS software, then those peaks assigned to Si can be reassigned to N atoms.

3.5.1.3 Decomposition

Atom Probe Tomography offers high spatial resolution, high analytical sensitivity (as high as 1 ppm) over volumes of greater than 10^6 nm^3. The concentration of different elements in the nickle nitride is investigated by the ATP. Previous compositional study performed using the XPS showed that the nickel nitride thin films did not contain C and O at levels above the XPS detection limit of about 1 atomic %. As shown in Table, the concentration analysis by atom probe confirmed that the number of C and O atoms inside the DLE-CVD nickel nitride is less than 1% of all atoms.

Element	Atomic %
C	0.88
N	5.47
O	0.65
Ni	89.78
Si	3.22

Table 3.2. Concentration of various elements found in the ATP sample.

3.5.2 ATP result of NiN_x film inside and outside of ultra high aspect ratio nanostructures

3.5.2.1 ATP Sample preparation

APT specimens from both outside and deep inside the trench were acquired by the FIB lift-out technique, followed by annular milling with Ga^+ ion beam to sharpen the specimens into 50-100 nm needles with shank angles around of 10°. The FIB sample preparation process is illustrated in Fig3.8 First, a region contains one entire side of a trench, as is indicated by the box in Fig 3.9, is extracted and mounted on a flat-top silicon post. The upper side of the piece (referred as "outside specimen") is aligned with the center of the post and welded onto it by in-situ FIB deposition of tungsten metal. The extra part of the piece is then cut out and mounted onto another post, becoming the "inside specimen". Afterwards, these specimens were cut into pyramid shape and further sharpened into ultrasmall needles by annular milling. As shown in the SEM image Fig3.9, two tips from part A and Part B were made by FIB process. The diameters of the tips are around 40 nm which is much smaller than the PSM sample.

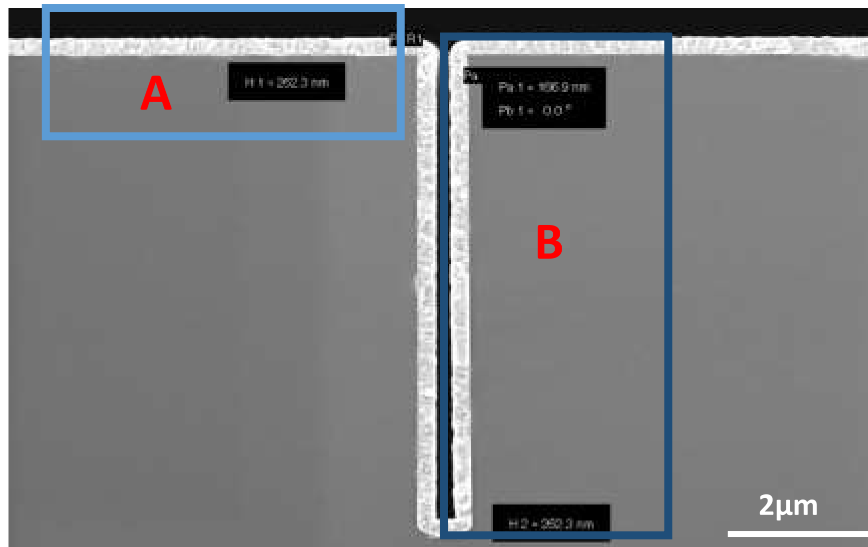


Figure 3.7. Cross sectional SEM micrograph showing the two regions from which the tips are made from using the FIB procedure

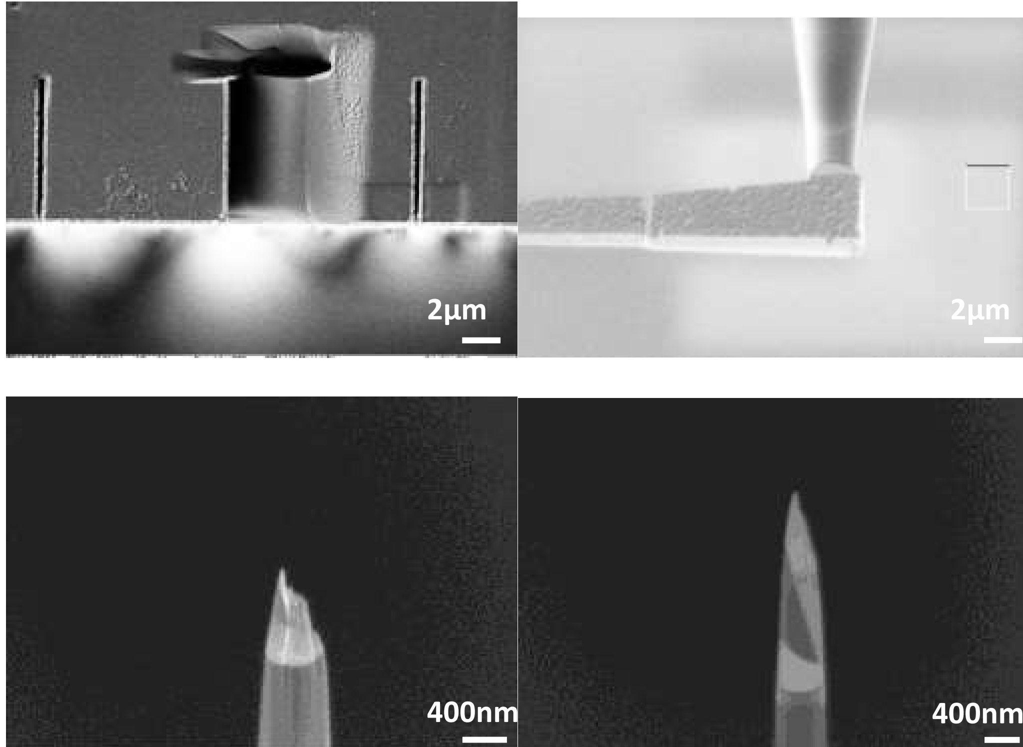


Figure 3.8. SEM micrograph of FIB processing for ATP sample and the ATP sample for NiNx from inside and outside of trench

3.5.2.2 Compositional depth profile of Nickel Nitride

Based on the mass spectra, compositional information was obtained from 10 nm diameter cylindrical regions perpendicular to the Ni nitride interfaces in the specimens both inside and outside trench. To avoid surface contamination and damage from the sample preparation processes, ~30 nm surface layers on the specimens were electrically evaporated before

recording ATP data, thus exposing the pristine bulk sample for analysis. The compositional depth profiles, as shown in Fig 3.10 are plotted from 30 nm to 100 nm along the specimens (0 nm denotes the top of the tip). From the results, more than 91% of Ni is observed along with 6% of N; the amounts of C and O are less than 3%. The compositions inside and outside the trench are almost the same.

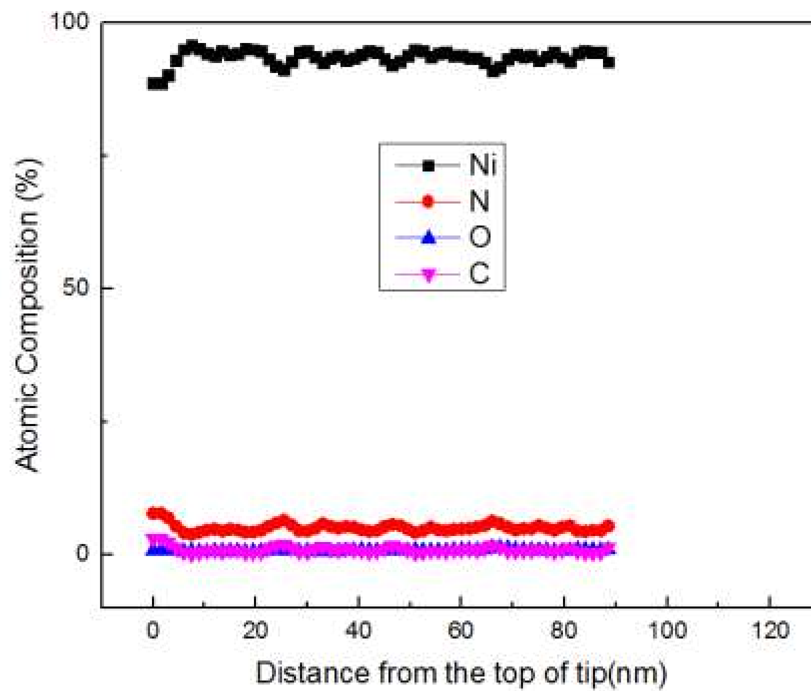


Figure 3.9. Compositional depth profile of an ATP sample from outside the trench, part A.

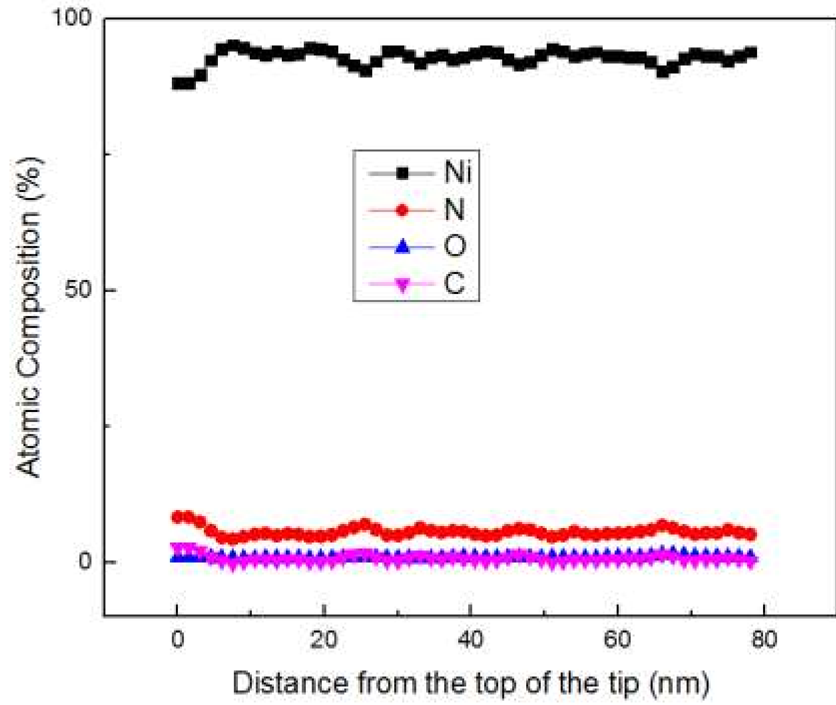


Figure 3.10. Compositional depth profile of an ATP sample from inside the trench, part B.

3.5.2.3 Spatial Compositional Mapping of NiN_x

Two APT analysis results of samples “outside trench specimen” and “inside trench specimen” are shown in Fig. 3.12 and Fig. 3.13. The analysis lengths of the outside and inside specimen are both 100nm. The large volume (30x30x100 nm^3) analyzed ensures that reliable statistical information is obtained from a single dataset. The two dimensional elemental maps of Ni, N, O and C atoms are shown in Fig. 3.12 and Fig. 3.13. The Ni, N, O and C atoms are represented by green, light green, white, and dark red colors respectively. The distribution and Ni and N atoms are highly uniform with no grain boundaries or clusters. The trace amounts of C and O are also uniformly distributed in the films.

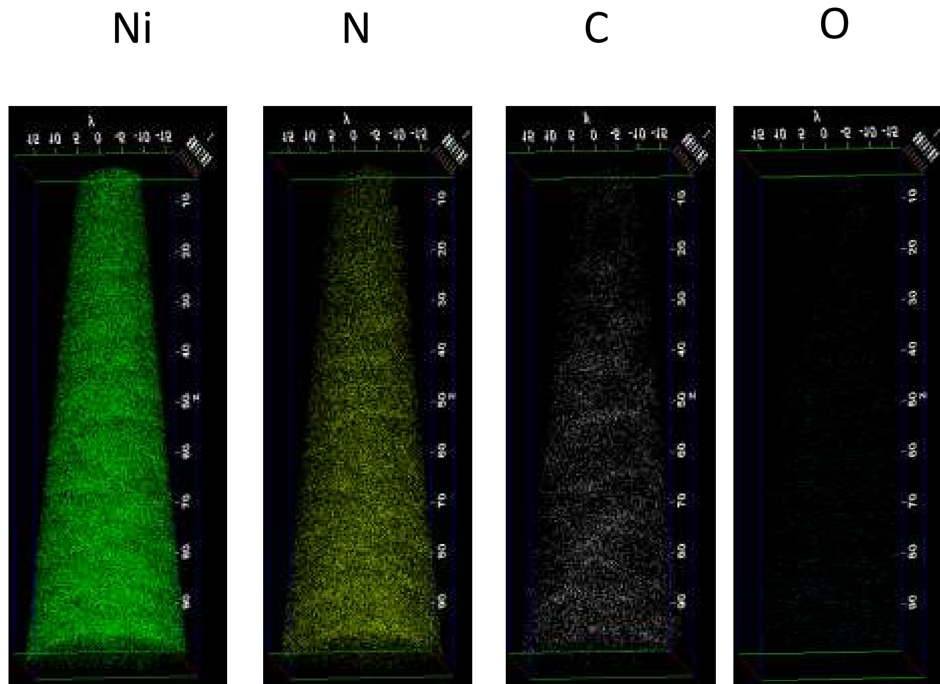


Figure 3.11. Spatial Compositional map an ATP sample from outside the trench, part A.

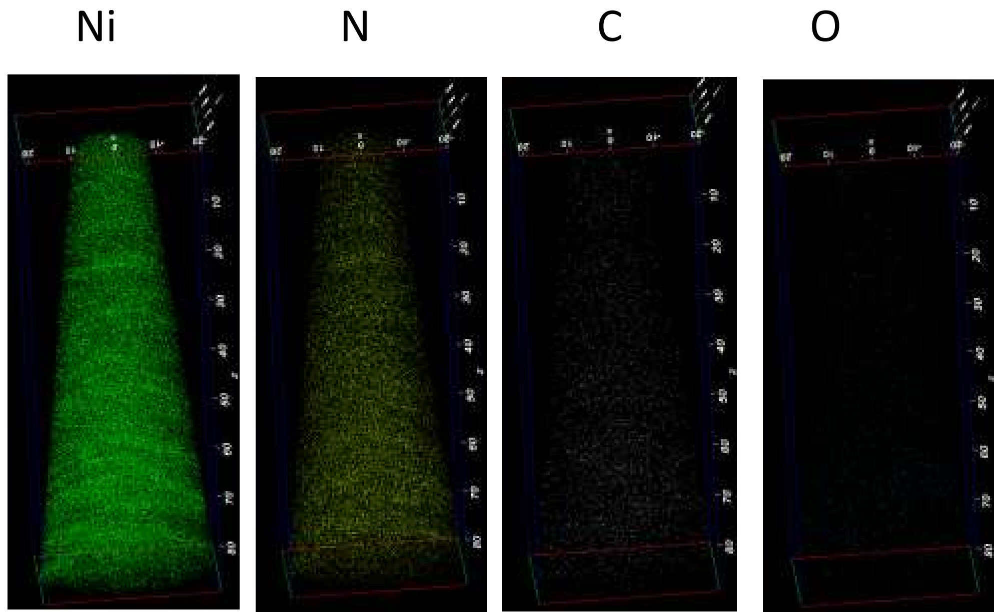


Figure 3.13. Spatial Compositional map an ATP sample from inside the trench, part B.2

3.6 Atom Probe Investigation of Nickel Silicide Thin Films in Ultra high aspect ratio nano structures

To analyze the Ni Silicide formed in the test structure, APT is adopted to provide high resolution three-dimensional compositional information.

3.6.1 ATP sample preparation

APT specimens from both outside and deep inside the trench were acquired by the FIB lift-out technique, followed by annular milling with Ga^+ ion beam to sharpen the specimens into 50-100 nm needles with shank angles around of 10°. The FIB sample preparation process is illustrated in Fig.3.14. First, one region containing one entire side of a trench, as is indicated by the white

dashed box in Fig.3.14, was extracted and mounted on a flat-top silicon post. The upper side of the piece (referred as “outside specimen”) was aligned with the center of the post and welded onto it by in-situ FIB deposition of tungsten. Then the extra part of the piece was cut out and mounted onto another post, becoming the “inside specimen”. These specimens were then cut into pyramid shapes and further sharpened into ultra-small needles by annular milling.

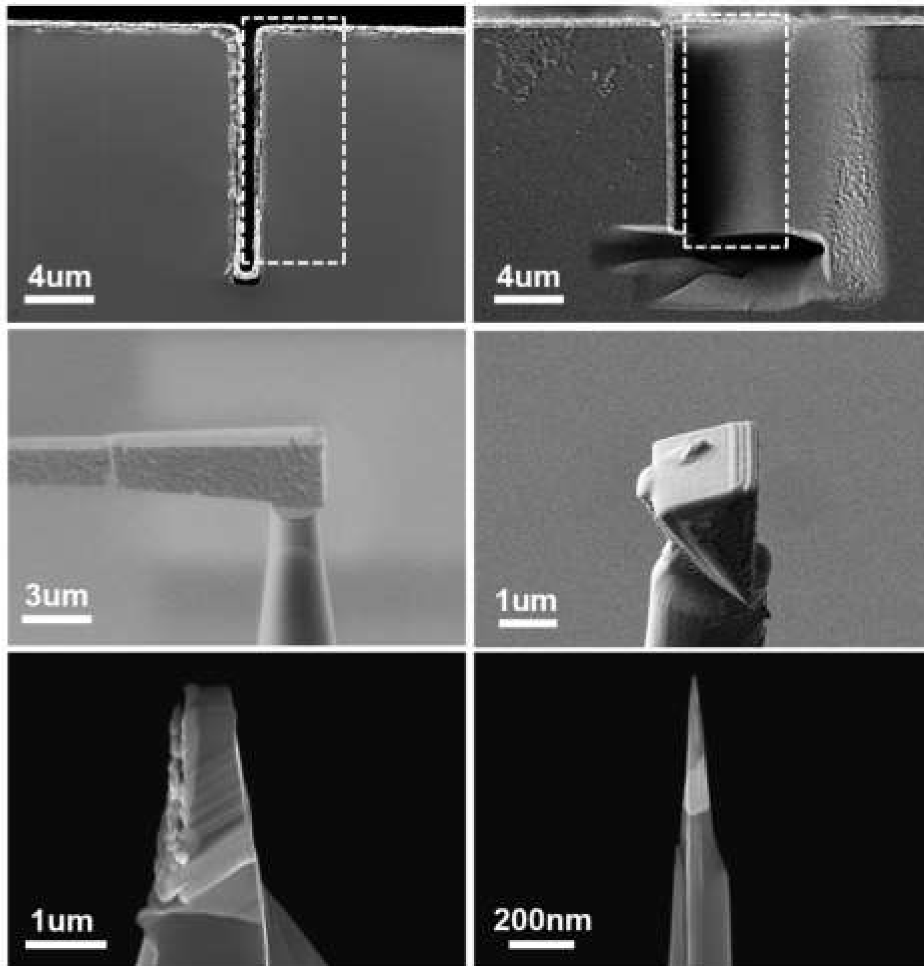


Figure 3.13. SEM images showing the process of creating an ATP specimen from a trench sample.

3.6.2 1D compositional depth profiles

Based on the mass spectra, compositional information was obtained from cylindrical regions 10 nm in diameter and perpendicular to the Ni silicide interfaces in the specimens from both inside and outside the trench. To avoid surface contamination and damage from sample preparation processes, ~60 nm of the surfaces of the specimens were electrically evaporated before recording ATP data, thus exposing the pristine bulk sample for analysis. 1D compositional depth profiles, as shown in Fig are plotted from 60 nm to 180 nm along the specimens (0 nm denotes the top of the tip). From the results, nearly equal amounts of Ni and Si (50% each) were observed, and considering that the distributions of Ni and Si are uniform, we thus conclude that the analyzed specimen is single-phased NiSi, rather than a mixture of different phases like Ni_2Si and $NISi_2$. Aside from Ni and Si, only less than 0.1% of O and C impurities were detected, which exhibits the ultrahigh purity of NiSi phase prepared by DLE-CVD process.

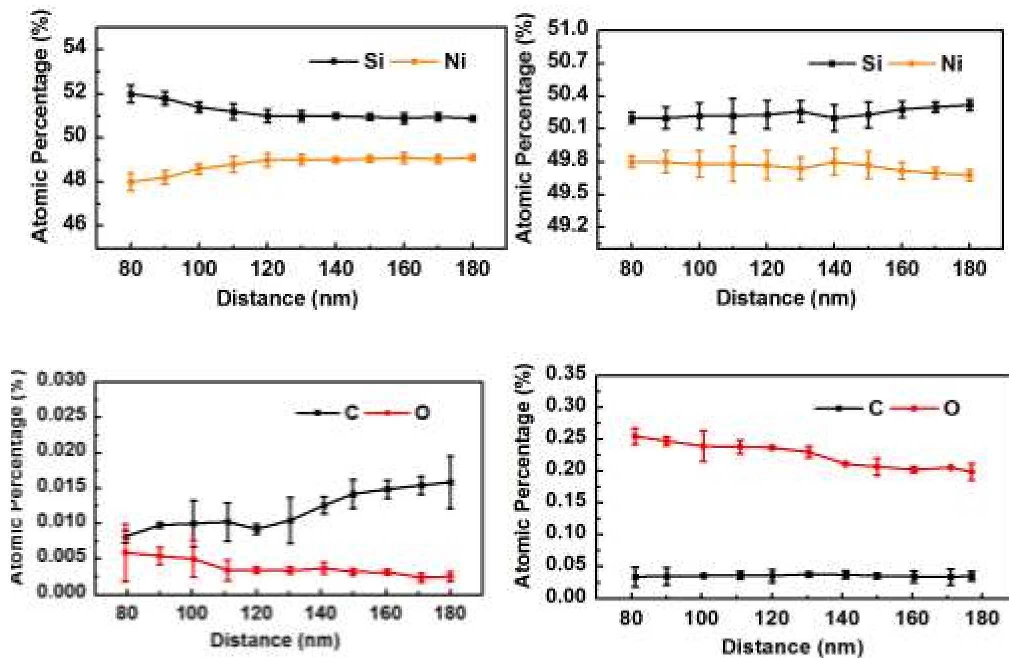


Figure 3.14. Compositional depth profiles of the barious elements in the NiSi ATP sample.

3.6.3 Spatial Composition Mapping of Nickel Silicide

Two APT analysis results from the “outside specimen” and “inside specimen” are shown in Fig 3.16. The analysis lengths of the outside and inside specimen are 200 nm and 360 nm presented in Fig, respectively. The large volume (40x30x200 nm3 and 50x30x360 nm3) analyzed in Fig. 3.16 ensures that reliable statistical information can be obtained from a single dataset. The two dimensional elemental maps of Ni and Si atoms are shown in Fig 3.16. The Ni and Si atoms are represented by blue and grey dots, respectively. The distribution and Ni and Si atoms are highly uniform with no grain boundaries or clusters.

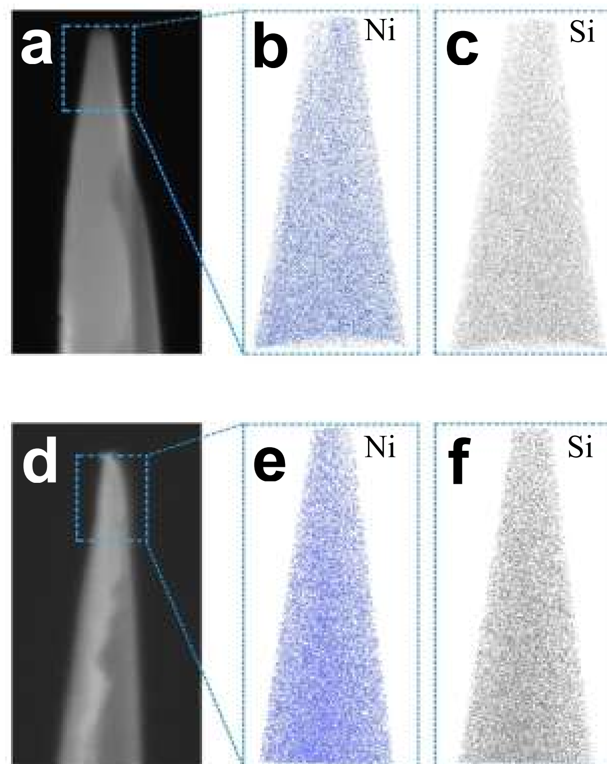


Figure 3.15. Spatial Compositional map of Ni and Si atoms in a specimen extracted from (top) the outside of the trench(a) (b) (c) and (d) (e) (f) from inside the trench.

3.6.4 Decomposition

The decomposition data process is conducted by IVAS process. The composition of all elements in the analyzed region of samples from inside and outside trench are listed in Table 3.3. The decomposition process decomposes complex ions such as SiO^+ and NiH^+ into single atoms, as well as differentiates the overlapped peaks such as Si^{2+} and N^+ by calculating the abundance ratios among different isotopes. The decomposition can only be computed with an adequate amount of statistical data; trace amounts of N were only observed in the decomposed composition results but not in the 1D compositional depth profile since the 1D profile is based on thin slices with small numbers of data points. Of note, the ultra-low concentrations of impurities are undetectable in most conventional elemental analysis methods, including XPS, RBS, EDX, XRF and EELS. Therefore, APT analysis offers the quantitative feasibility to characterize and even visualize trace amounts of impurities, which enables a feedback loop to fine-tune adjustments and make improvements in deposition techniques for thin films.

	Outside Trench	Inside Trench
Element	**Atomic Percentage (%)**	**Atomic Percentage (%)**
Ni	**52.00 ± 0.03**	**50.12 ± 0.05**
Si	**47.87 ± 0.10**	**49.83 ± 0.09**
C	**0.02 ± 0.01**	**N/A**
N	**0.04 ± 0.02**	**0.03 ± 0.02**
O	**0.07 ± 0.03**	**0.015 ± 0.005**

Table 3.3. Elemental composition of the various elements in the outside and inside trench specimen

3.7 Conclusions

This chapter successfully demonstrated that ATP analysis can be effectively applied to the understanding of the microstructure and compositional properties in thin films. The validity of the technique has been proved by the application of APT for nickel nitride and nickel silicide films. PSM and FIB specimen preparation methods have been applied and their pros and cons have been discussed. The impact of different parameters in ATP analysis has been investigated using DLE-CVD Nickel Nitride PSM specimens. The composition analysis of DLE-CVD Nickel Nitride and Nickel Silicide thin film inside and outside of high aspect ratio (1:10) trench structures has been conducted through ATP analysis with FIB-prepared specimens. Leveraging the highly conformal depositions using the DLE-CVD technique, compositional uniformity was achieved on specimens both on the inside and the outside of trenches. From the ATP results, 1:1 Ni-to-Si atomic ratio and highly uniform distribution of both Ni and Si was observed, indicating the formation of single-phase NiSi. The high resolution of ATP provides the capability of counting and localizing trace amount of impurities (~0.1% in total), which are conventionally undetectable by most elemental analysis techniques.

The results also demonstrate the DLE-CVD of Ni and its conversion to NiSi as a highly promising approach for the semiconductor industry to overcome the current obstacles on interfacial issues for silicon contacts. The outstanding capability of ATP at detecting ultra-low

concentration of impurities also offers a guidance to design and realize better functional materials for modern semiconductor industry.

References

[42] J. J. Determination, Y. Wu, J. Xiang, C. Yang, W. Lu, and C. M. Lieber, “Single-crystal metallic nanowires and metal / semiconductor nanowire heterostructures,” vol. 717, no. 1992, pp. 334–338, 2004.

[43] S. Kim and O. Song, “Properties of Nickel-Cobalt Composite Silicides by Thermal Annealing and Polysilicon Substrates,” vol. 13, no. 3, pp. 239–247, 2007.

[44] D. Mangelinck, K. Hoummada, F. Panciera, M. El Kousseifi, I. Blum, M. Descoins, M. Bertoglio, A. Portavoce, C. Perrin, and M. Putero, “Progress in the understanding of Ni silicide formation for advanced MOS structures,” *Phys. Status Solidi Appl. Mater. Sci.*, vol. 211, no. 1, pp. 152–165, 2014.

[45] R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, “Integrated nanoelectronics for the future.,” *Nat. Mater.*, vol. 6, no. November, pp. 810–812, 2007.

[46] A. Franco, J. Geissbühler, N. Wyrsch, and C. Ballif, “Fabrication and characterization of monolithically integrated microchannel plates based on amorphous silicon,” *Sci. Rep.*, vol. 4, no. August 2015, pp. 1–7, 2014.

[47] Z. Li, R. G. Gordon, V. Pallem, H. Li, and D. V. Shenai, “Direct-liquid-injection chemical vapor deposition of nickel nitride films and their reduction to nickel films,” *Chem. Mater.*, vol. 22, no. 10, pp. 3060–3066, 2010.

[48] H. Takamizawa, Y. Shimizu, Y. Nozawa, T. Toyama, H. Morita, Y. Yabuuchi, M. Ogura, and Y. Nagai, “Dopant characterization in self-regulatory plasma doped fin field-effect transistors by atom probe tomography,” *Appl. Phys. Lett.*, vol. 100, no. 9, 2012.

[49] T. F. Kelly, D. J. Larson, K. Thompson, R. L. Alvis, J. H. Bunton, J. D. Olson, and B. P. Gorman, “Atom Probe Tomography of Electronic Materials,” *Annu. Rev. Mater. Res.*, vol. 37, no. 1, pp. 681–727, 2007.

Chapter 4 DLE-CVD manganese-based and CuMn alloy thin film materials for interconnects in 3D microprocessors

4.1 Introduction

Continuous enhancements in device performance and functionality have been achieved via the reduction in the physical size of devices and by increasing the number of levels of metal wirings. However, many challenges arise from the shrinkage of device sizes, which casts doubts about the sustainability to the “Si Revolution”.[50]

Metal interconnections in microelectronics have been typically fabricated in a planar, 2-dimensional (2-D) fashion. 3-dimensional (3-D) integration has garnered a large amount of interest as a solution to enhance the performance of microelectronic systems. 3-D integration can reduce the number and the average lengths of 2-D wires by providing shorter vertical paths. In addition, 3-D integration has the potential to improve system performance and to enable new system architectures. 3-D integration also offers the possibility to integrate dissimilar technologies, such as digital, analog, and radio-frequency (RF) functions, all in the same system for system-on-chip (SOC) applications.

The continuation of the Si revolution will rely on the advancements of both the 3D transistors and 3D integration as mentioned by Liu .[51] 3D transistors have been discussed in Chapter 3.

For 3D integration, the interconnects are crucial. The 3D transistors are connected to the global interconnects via the local interconnects, and the global interconnects connects all the different layers together. With the increasing packing density inside the integrated circuit, the critical dimension is shrinking to sub 20 nanometers. For such small features, the industry is working on replacing the traditional copper electroplating processes in the dual-damascene with vapor deposition. This is necessary for filling the sub-100 nm trenches that have aspect ratios greater than 3:1 as traditional PVD methods are unable to meet these high requirements as Fig 4.1 shows.

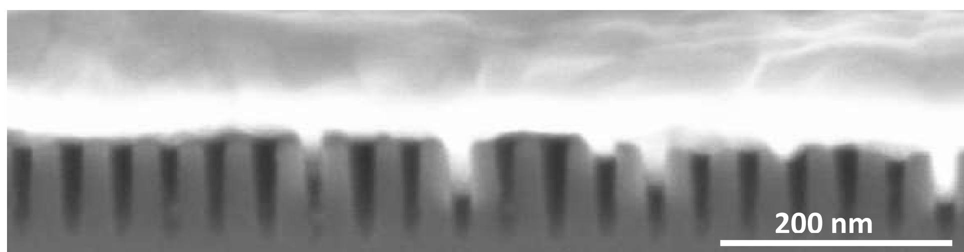


Figure 4.1. PVD Cu film on the sub-50 nm trenches [41]

Iodine adsorbed on a copper seed layer has been shown to act as a catalytic surfactant [11] that is able to improve growth rate and surface smoothness of copper films deposited by DLE-CVD. During iodine-catalyzed DLE-CVD in sub-100 nm trenches, the growth rate of copper at the bottom of the features is continuously accelerated due the reduction of surface area and increasing concentration of iodine catalyst. As a result, bottom-up filling of copper was achieved as shown in Figure 4.2. This catalyst-enhanced process requires a conformal copper seed layer on top of the diffusion barrier and adhesion layer. Preparation of this seed layer is challenging on sub-30 nm features.

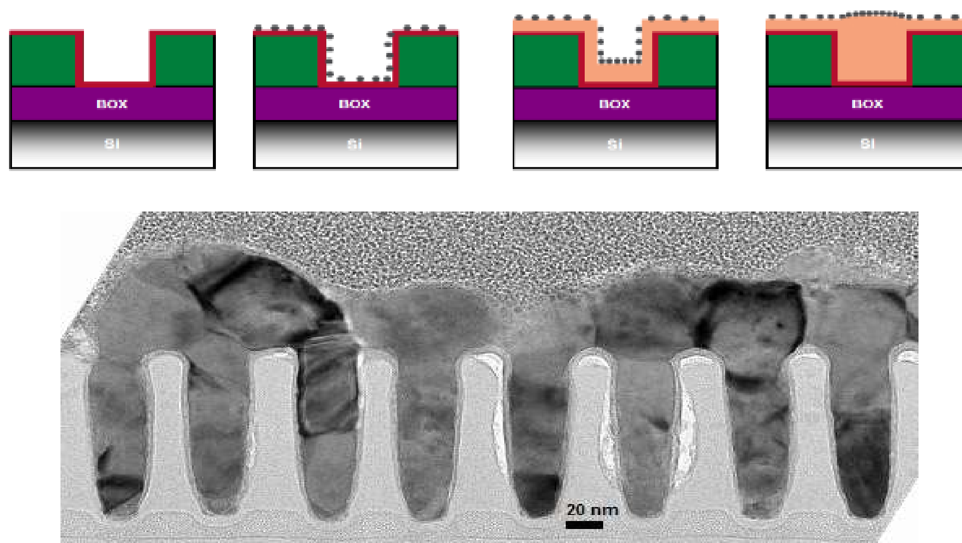


Figure 4.2. Iodine surface catalyzed bottom-up filling ultra-narrow trenches. (source: IBM collaboration and [41])

3D integration includes two different aspects: 3D transistor stacking and heterogeneous integration.[2] The 3D transistor stacking involves a stack of several layers of transistor in a single chip, which have a much higher transistor density than a single layer transistor, such as the 3D NAND flash technology where polycrystalline Si is used as the semiconductor material. However poor heat dissipation imposes a limitation to the application of 3D transistor stacking in the semiconductor industry. [52]

Heterogeneous Integration refers to the integration of different functionalities in a single package.[51] The enables the enhancement of performance in a compact form factor, making the system more power efficient. This allows significant miniaturization of the product sizes as well bring about considerable cost reductions.

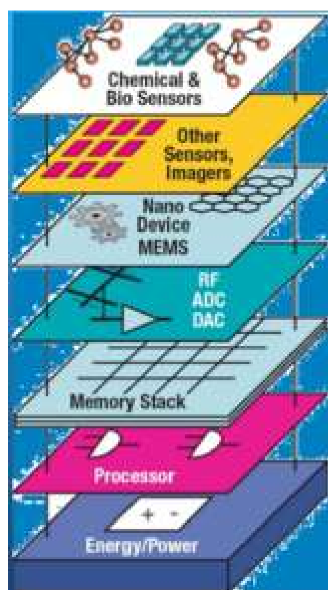


Figure 4.3. Heterogeneous Integration of multifunctional chips (source: www.monolithic3d.com)

Modifying the processes used in separate layer fabrication into one for integrated fabrication processes is highly challenging. Three dimensional silicon integration of active devices with through-silicon vias (TSVs), thinned silicon and silicon-to-silicon fin pitch interconnects offers many benefits. TSVs has so far been the most promising method favored by the industry. [53]While TSVs will provide faster interconnections between multiple dies in advanced 3D-packaging applications, the metallization of TSVs will become more and more difficult as the aspect ratios of these vias continue to increase. [54] One critical step in the production of TSVs is the preparation of a continuous barrier that will keep metals from diffusing out from the vias. A smooth and conductive copper seed layer is also necessary to initiate copper electroplating. Strong adhesion must also be provided between the copper seed layer, the diffusion barrier and the underlying dielectric. Due to their poor step coverage, conventional physical vapor

deposition (PVD) methods will no longer to be able to cover the sidewalls of these high aspect ratio features with the necessary layers as shown in Fig 4.4.[55] As we increase the number of integration on each layer, the density of TSVs also increase dramatically. Even bubbler based CVD MnN_x and CVD copper process can no longer fully cover the bottom of the TSVs shown as Fig 4.5 due to insufficient supply of precursors in the traditional bubbler based CVD processes.

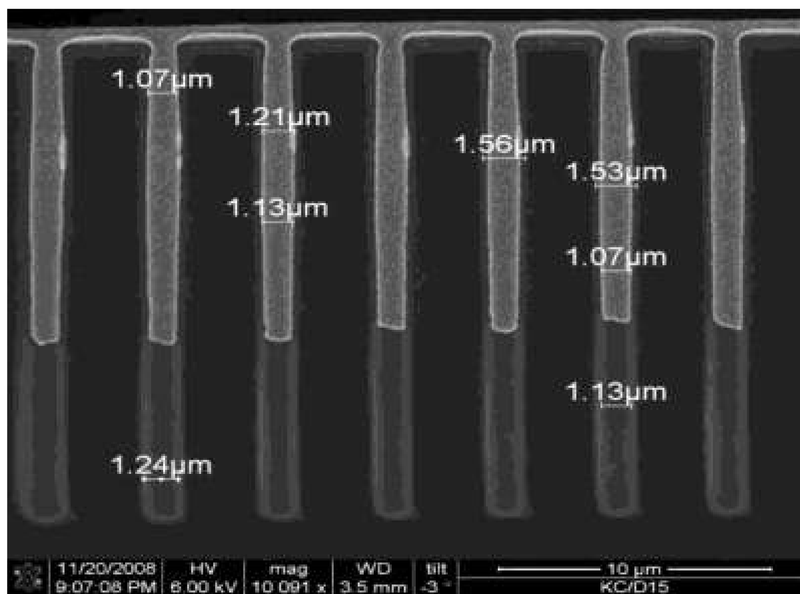


Figure 4.4. PVD Cu for TSV with 1 to 20 aspect ratio [55]

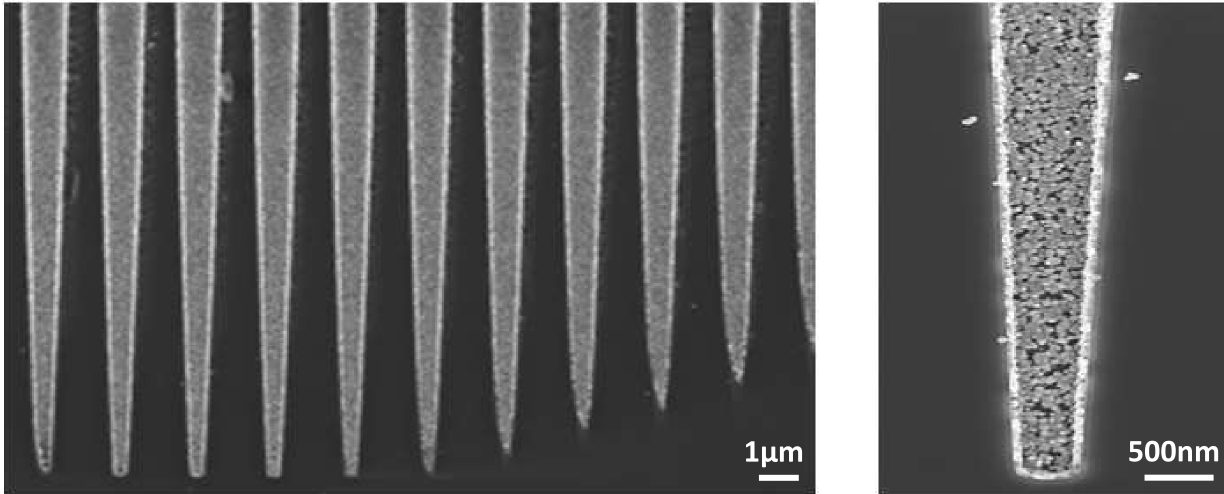


Figure 4.5. Cross-sectional SEM images depicting how high density TSVs can not be fully covered by the traditional bubbler based CVD processes. [41]

In this chapter, we discuss the DLE-CVD deposition of conformal, smooth and strongly adherent barriers and copper coatings inside very narrow trenches (sub-100 nm) and TSVs with aspect ratios greater than 25:1. Manganese nitride (MnN_x), an effective copper diffusion barrier and adhesion layer, is deposited conformally by DLE-CVD on its substrates. Iodine is able to be chemisorbed onto the surface of a thin, conformal manganese nitride layer. When the DLE-CVD of copper begins, the iodine is first released from the surface of the manganese nitride. The iodine then floats on the surface of a growing copper layer and catalyzes the bottom-up filling of trenches without leaving any seams or voids. Manganese is co-deposited with copper film through a DLE-CVD process to get a CuMn alloy film, which is used to enhance the adhesion strength between the CuMn alloy film and the dielectric substrate. A post-deposition annealing step allows manganese to diffuse from the copper film to the surfaces of the insulators to strengthen further the copper/dielectric interface by forming a self-aligned barrier as well as an adhesion layer. Using this procedure, sub-100 nm trenches and TSVs are provided with

conformal and smooth CuMn alloy seed layers that adhere strongly to a very thin diffusion barrier just inside the surface of the conformal silica insulator.

4.2 Experiments

Deposition of manganese Nitride, copper-manganese Alloy Films on sub 100 nm patterned substrates with trench structures and TSVs

Patterned silicon substrates with narrow trenches were obtained from IBM that has a critical dimension (CD) of sub 50 nm and an aspect ratio of about 3:1. These substrates are first cleaned using an UV/ozone cleaner (Samco model UV-1, wavelengths = 185 nm and 254 nm) for 5 minutes at room temperature to remove organic contaminants from the substrates.

Manganese nitride was deposited via the DLE-CVD process at 130 ^{o}C for only 3 minutes as discussed at Chapter 2. Since the width of trench is quite narrow, when using manganese nitride as an adhesive and barrier layer, it must be as thin as possible to leave more space for copper fillings. For the substrates with narrow trenches, a special surfactant-catalyzed process was applied to achieve bottom-up and void-free filling of the trenches.

Ethyl iodide (CH_3CH_2I) was then used as an iodine source to adsorb atoms onto the fresh surface of the manganese nitride film at 50 ^{o}C. The ethyl iodide liquid was contained in a

bubbler at room temperature and its vapor flew directly into the reactor without a carrier gas, controlled by a needle valve to a pressure of 0.05 Torr.

The Cu-Mn alloy film is deposited using the DLE-CVD CuMn alloy process at 180 ^{o}C as discussed previously in Chapter 2. In a typical process that the trenches are filled with CuMn alloy, manganese nitride was first deposited at 130 ^{o}C for 3 minutes to form ~3 nm layer of film. Ethyl iodide was then introduced into the chamber at 50 ^{o}C for 30 seconds. DLE-CVD CuMn was then deposited at 180 ^{o}C until the trenches are completely filled. Then the sample was post annealed at 350 ^{o}C for 2 hrs.

Patterned silicon substrates with TSV features were obtained from Applied Materials (AMAT). These substrates were cleaned by a UV/ozone cleaner (Samco model UV-1, wavelengths = 185 nm and 254 nm) for 5 mins at room temperature to remove organic contaminants from the substrates.

In a typical DLE-CVD process used to form CuMn alloy seed layers in TSV features, approximately 20 nm of silica layer was first deposited by ALD at 250 ^{o}C to insulate the metal from the silicon. Manganese nitride was then deposited at 160 ^{o}C for 10 minutes to form 15 nm of film. Copper-manganese alloy was deposited at 200 ^{o}C until a sufficiently conductive layer (sheet resistance below 0.8 ohms per square) was formed in the vias.

Characterization Method

The thickness of MnN_x and CuMn alloy films was measured by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). The effectiveness of manganese nitride as a barrier to copper diffusion was tested by looking for its reaction with silicon to form copper silicide under an energy-dispersive X-ray spectrometer (EDX) and TEM. The effectiveness of manganese nitride as an adhesion layer was evaluated using the tape test method.

The effectiveness of DLE-CVD copper in super-filling narrow trenches was evaluated by cross sectional SEM and TEM. The cross sectional SEM and TEM samples were prepared by Focused Ion Beam (FIB). The Mn/Cu ratio was quantified by X-Ray Fluorescence (XRF).

Samples prepared for electrical characterization at IMEC received an additional 300 nm of thermally evaporated copper to make them more suitable for chemical-mechanical polishing(CMP). The samples were then post-annealed at 300 ^{o}C for 2 hours under nitrogen gas ambient to diffuse the manganese from the alloy to the copper/dielectric interface. Following CMP, the resistivity values of the copper wires were determined by electrical measurements. In the TSVs, the conformity of MnN_x and CuMn seed layers were evaluated using SEM.

4.3 Results and Discussion

Barrier and Adhesion Properties of manganese Nitride Films

Manganese nitride films has been shown to exhibit properties of an excellent barrier against copper diffusion. For this copper diffusion test, DLE-CVD manganese nitride fabricated at 130 ^{o}C for 10 minutes was deposited on SiO_2 substrates. A layer of copper film of about 70 nm thick was then deposited on top of the manganese nitride layers. The samples were then annealed in a pure nitrogen atmosphere at 400 ^{o}C for 1 hour. To determine whether copper had diffused into the silicon substrate, the sample was analyzed by cross-section TEM and EDX, giving the results as shown in Figure 4.6. The control experiment has been done by several other groups which all showed that copper will diffuse into silicon to form copper silicide crystallies without barrier layer. The manganese nitride treated sample does not show any copper in the silicon regions when analyzed using EDX, demostrating that MnN_x is an effective barrier against the

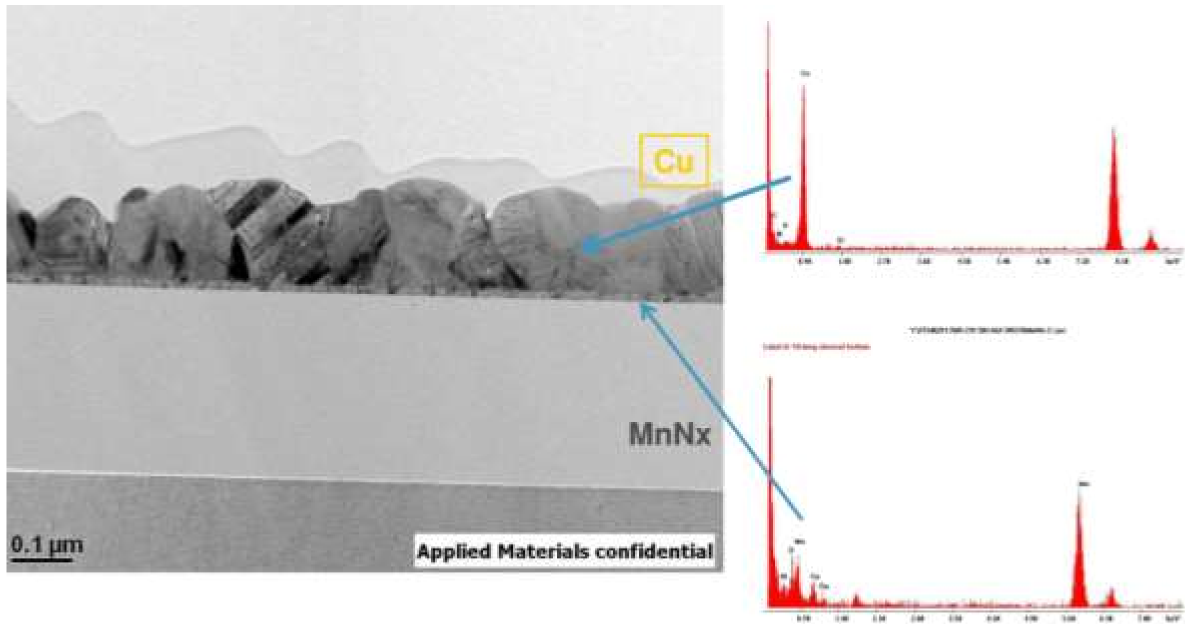


Fig 4.6. Cross Section TEM of annealed DLE-CVD Cu film on DLE-CVD MnNx, EDX on Cu film and MnNx film Source: Applied Materials Collaboration

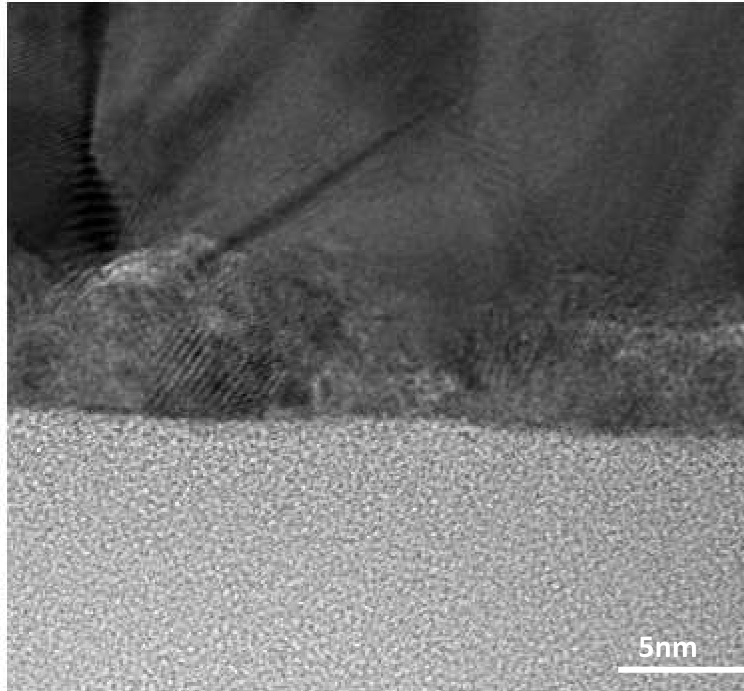


Figure 4.7. Cross-secional TEM image of the DLE-CVD MnNx film Source: Applied Materials Collaboration

The motivation to test the adhesion strength of planar copper films grown on manganese nitride is because the electromigration lifetime depends on the adhesion strength of the copper with surrounding material. The tape test is a standard test widely utilized by the industry for this purpose. After depositing 3 nm of manganese nitride and 60 nm of copper, the structures were tested and successfully passed the tape test.

Bottom-up filling of Sub-100nm Treches by Surfactant-Catalyzed DLE-CVD of CuMn alloy

Narrow trenches can be filled by CuMn alloy in a bottom-up style without leaving any voids or seams when manganese nitride film of approximately 3 nm is used as the underlayer and iodine is used as the surfactant catalyst. TEM analysis showed the complete filling of the trenches with copper, which were around 36 nm wide and 100 nm deep giving it an aspect ratio of 3:1. There are no voids and seams along the walls of the trenches. The fact that the CuMn alloy grew faster from the bottom than from the sides of the trenches suggests that iodine pre-adsorbed on the MnNx was released from the MnNx layer and then catalyzed the bottom-up filling of these trenches as a surfactant floating on the growing surface of the CuMn alloy.

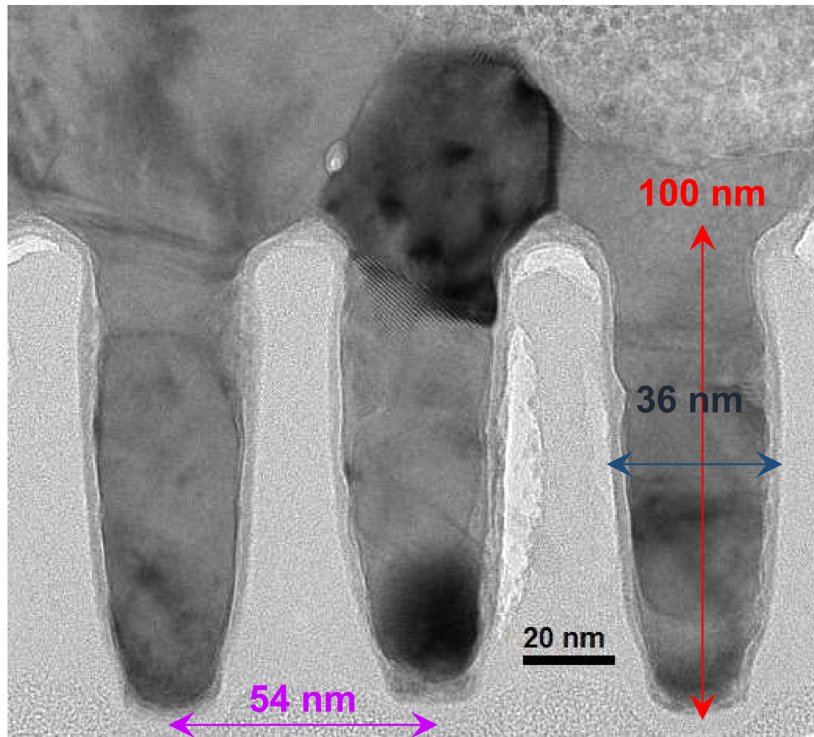


Figure 4.8. Cross Section TEM images of DLE-CVD Copper filled ultra-narrow trenches source: IBM Collaboration

Electrical Characterization of Narrow Trenches filled with DLE-CVD of Cu-Mn alloy

Manganese was incorporated into the DLE-CVD copper process to form CuMn alloy, which was analyzed by XRF to have approximately 1%-2% atomic percent of manganese in copper. The trenches were completely filled with the CuMn alloy.

Upon annealing at temperatures above 350 ^{o}C, manganese diffuses through the grain boundaries of copper to the surfaces of the dielectric layers. The diffusion process returns the

resistivity of copper to the same magnitude of its original value and also strengthens the copper/dielectric interface by firming a self-aligned barrier and adhesion layer at the interface. When the ratio of manganese to silicon bonds exceeds about 0.5 at the interface between the Cu-Mn and the dielectric, the de-bonding energy becomes larger than about 15 J per square meter. [41]This very strong adhesion is expected to greatly increase the lifetime of copper interconnects before they fail by electromigration.

For the CuMn alloy filled with different critical dimension of narrow trenches (20nm-140nm). Chemical Mechanical Polishing (CMP) process was used to remove PVD Cu at the top of the trench as shown in Figure 49. Figure 4.10 shows that resistivity values measured on trenches with 20, 60, 100 nm critical dimension which are quite similar with conventional PVD RuTa liner/electroplated Cu method.

Although the increase of Mn atomic concentration may cause an increase in the resistivity, the DLE-CVD CuMn alloy method incorporated less carbon, oxygen, and other impurities into the copper film than conventional electroplating methods, which reduces impurity scattering. On the other hand, the post-annealing step following the DLE-CVD process promotes CuMn alloy grain growth, which aided in reducing grain boundary scattering. These effects combined to result in lower resistivity values.

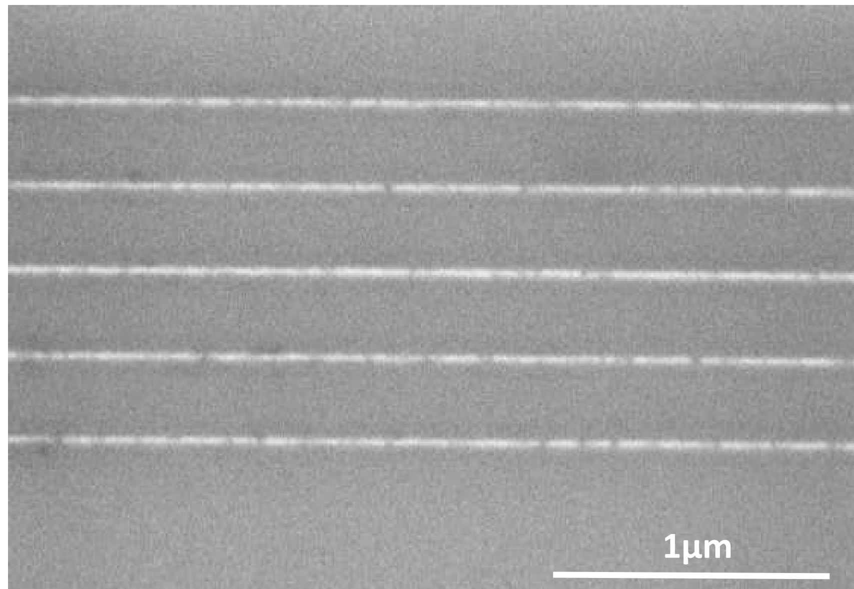


Figure 4.9. Sub-100 nm trenches filled with the Cu-Mn alloy material after CMP to prepare for electrical measurements. Source: IMEC Collaboration

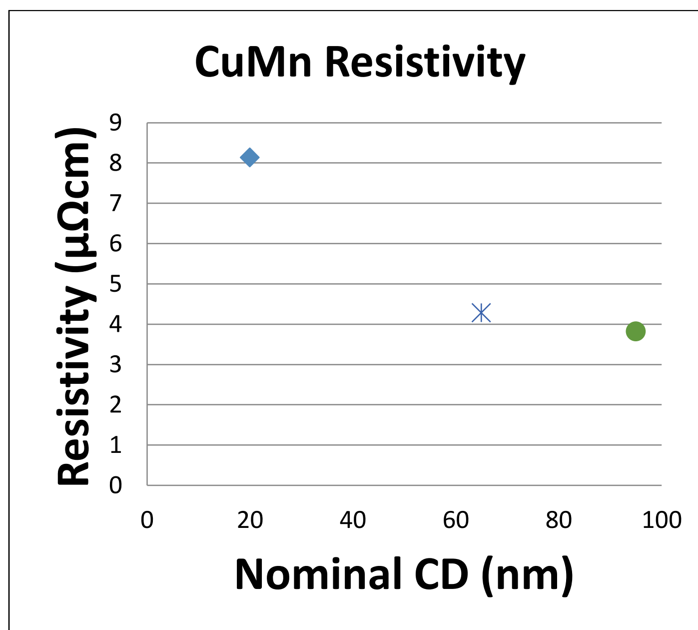


Figure 4.10. Resistivities of the CuMn material used to fill in trenches with different CDs Source: IMEC Collaboration

Conformal Copper Seed Layers for Plating Through-Silicon Vias (TSV)

An ALD silica layer is first deposited in the TSV holes with aspect ratios of 25:1 to create a clean surface. A MnN_x layer is deposited next using the DLE-CVD process carried out at 160 ^oC for 10 minutes which correspond to a film thickness around 15 nm. As discussed in Chapter 2, the DLE-CVD MnN_x process can cover the vias with aspect ratio as high as 50:1.

DLE-CVD CuMn process delivers a much higher partial pressure of the precursor vapor than the traditional bubbler based CVD process. By supplying a high concentration of copper precursor vapor, the deposition operates in the surface reaction-controlled regime. At deposition temperatures of around 200 ^oC, an uniformly high concentration of copper and manganese precursor vapor is delivered to the entire length of the vias. As a result, continuous and highly conformal CuMn alloy films are deposited on MnNx underlayers inside via holes with aspect ratio over 25:1. The vapor delivery rate from the DLE system is stable, reproducible and accurately known because the concentration of the solution and the liquid and carrier gas injection rates are known and steady. In contrast, the vapor delivery rate from a conventional bubbler is subject to uncertainties in vapor pressure, temperature variation, and thermal decomposition.

Cross section SEM images of the TSVs with aspect ratio 25:1 is shown in Fig 4.11, showing the continuous and highly conformal copper films deposited on the MnNx underlayers inside via holes with aspect ratio over 25:1.

DLE-CVD CuMn alloy can be used to enhance the adhesion between the seed layer to the dielectric layer. A post-deposition annealing step at 350 ^{o}C is incorporated to cause the diffusion of manganese from CuMn alloy layer to the copper/dielectric interface. The manganese diffuses through the grain boundaries of the polycrystalline copper, and this diffusion enhance the interfacial adhesion between copper and dielectrics such as silicon oxide, low-k dielectric. Manganese nitride provides sufficient adhesion energy to survive chemical-mechanical polishing.

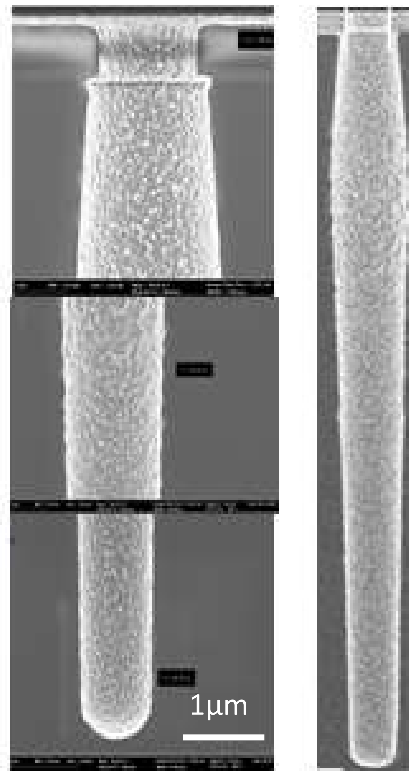


Figure 4.11. Cross Section SEM of TSV with DLE-CVD CuMn alloy film

Preliminary Electroplating Results

TSV features with aspect ratio of 25 to 1 (supplied by Applied Materials) were conformally coated with approximately 90 nm of Cu-Mn alloy seed layer as shown in Figure 4.12. Preliminary copper electroplating studies were carried out on these substrates at Dow Chemical Company, following the interlink 9200 TSV chemistry. The plating solution contained copper sulfate ($CuSO_4$)/sulfuric acid-based electrolytes and additives including an accelerator and a leveler to achieve bottom-up filling and to control the morphology of the electroplated copper. As shown in Figure 4.12, void-free TSV filling was achieved across all sections of the via arrays after 30 minutes of electroplating.

Figure 4.12. Cross-Sectional images demonstrating complete filling of high aspect ratio TSVs Source: Collaboration with Dow Chemical

4.4 Conclusions

As the density of 3D transistors increase, these electronic systems demand a higher density of trenches where the trenches are increasingly narrower than before, resulting in high aspect ratio structures that requires DLE-CVD for achieving highly conformal and continuous coatings for the fabrication of the TSVs needed to connect the layers together in the 3D architecture. DLE-CVD provides the capability of bottom-up filling of narrow trenches (under 30 nm diameter with aspect ratios as high as 5:1) with Cu or Cu-Mn alloy using MnNx underlayers and iodine as a surfactant catalyst. The presence of manganese at the copper/dielectric interface further improves the adhesion and the barrier properties at this interface. The DLE-CVD process forms a highly robust and conductive seed layer for the metalizing of future generations of copper vias for application in advanced 3-D integration. TSV features with aspect ratio of up to 25 to 1 can be completely filled using the Dow Chemical's electroplating processes. The DLE-CVD

method has been demonstrated to have enhanced the delivery of precursor vapors even to the bottoms of dense arrays of vias and resulted in near-perfect conformality.

References

[50] H. Havemann and J. A. Hutchby, "High-performance interconnects: An integration overview," *Proc. IEEE*, vol. 89, no. 5, pp. 586–601, 2001.

[51] T. Jae and K. Liu, "Sustaining the Si Revolution : From 3D Transistors to 3D Integration Impact of Moore ' s Law," 2015.

[52] Y. Madhour, "3D integrated architectures for microelectronic two-phase flow cooling applications," vol. 6323, 2014.

[53] A. Pil-Ali and M. A. Karami, "Through silicon via based metal-semiconductor-metal photodetector in CMOS technology," *Opt. Quantum Electron.*, vol. 48, no. 1, p. 13, 2016.

[54] E. C. S. Transactions and T. E. Society, "Analysis of high aspect ratio Through Silicon Via (TSV) diffusion and stress impact profile during 3D advanced integration L. Djomeni," vol. 61, no. 3, pp. 219–226, 2014.

[55] S. Armini, Z. El-Mekki, K. Vandersmissen, H. Philipsen, S. Rodet, M. Honore, a. Radisic, Y. Civale, E. Beyne, and L. Leunissen, "Void-Free Filling of HAR TSVs Using a Wet Alkaline Cu Seed on CVD Co as a Replacement for PVD Cu Seed," *J. Electrochem. Soc.*, vol. 158, no. 2, p. H160, 2011.

Chapter 5 Metallization on Polyaramids for electronic textiles with DLE-CVD Manganese and CuMn alloy thin film materials

5.1 Introduction

Electronic Textiles (e-textiles) refers to fabric materials that are embedded with electronics connected together via interconnections, enabling smaller sizes and greater flexibilities far beyond what can be achieved using traditional manufacturing techniques for electronics, which in turn allows these electronics to be highly aware of their environment and react swiftly to any changes it senses. [8]

Wearable systems are driving exciting, innovative applications in the health, wellness, safety and entertainment markets. As the user experience matures, not only is the product design following the latest fashion trends but also the practical factors such as function and fit. The human-centric element has created a paradigm for the interconnect designers and fabricators. It must survive continuous dynamic stresses brought on by flexing, bending, twisting, stretching and dropping in an uncontrolled use environment.[56] Communicating between different chips in wearable system are made possible via the use of robust tiny wiring between the different components. Separate sensors could be attached to a central communications chip, and combined with a solar cell to power them. More robust and economical methods for flexible connection of signals and power between separate chips would enable integration of these separate components into even more powerful systems. [57]

All these requirements can be satisfied by several solutions. Metal wires are one of the most commonly used materials, having the advantages of strength, composition, biological inertness and ready availability in textile form at low costs. However, their brittle characteristics can inflict damage to spinning machinery over time. Additionally, homogenous textile fiber blends are challenging to be fabricated, as they are heavier than most other textile fibers. Direct printing of conductive tracks on fabrics, although a technique that lends itself easily to being produced in large quantities, typically uses silver as a filler for these conductive inks making them brittle.[58] Such conductive inks are subjected to variations in its resistivity from crease formations too. [59] These reasons make treated coatings attractive as materials for interconnects in wearable systems as they are suitable for many types of fibers and demonstrate excellent electrical conductivity without the need to make significant changes to the fiber's material properties such as flexibility and density. Hu et al. leveraged a simple "dipping and drying" process using single-walled carbon nanotube ink to successfully produce highly conductive textiles with conductivities of 125 S.cm-1.[60] However, poor adhesion between the metal and the fibers as well as corrosion resistance can lead to problems when implemented in wearables.

In this chapter, we will discuss about the required strength, flexibility and electrical conductivity because of being combined in fibers built on polymers with high strength and good thermal

stability, such as polyaramids (Kevlar, Nomex or Zylon). For example, the decomposition temperature of Kevlar is around 427 ^{o}C in air and 538 ^{o}C in nitrogen.[61] Conformal, smooth and strongly adherent MnN_x and copper-manganese alloy layer can be coated on the Kevlar fibers with diameter around 11 um by using a DLE-CVD process. A rapid ALD process of aluminum-doped silicon dioxide was then applied at a substrate temperature of about 250 ^{o}C to electrically insulate to the wires. This tiny wire can also support more than a kilogram force without breaking. In a durability test in our laboratory, a wire was bent to a radius of 5 mm and then straightened more than half a million times without changing the electrical resistance of the wire.

5.2 Experiment

Deposition of manganese Nitride, copper-manganese alloy Films on Nomex fiber sheet and Kevlar fibers

Commercial available Nomex fiber sheet paper and Kevlar fiber were obtained from the DuPont company. The fibers are baked in an oven at 200 C to remove moisture and cleaned by UV/ozone for 5 minutes at room temperature to remove surface contaminants.

As an adhesion-promoting layer, manganese nitride was deposited on the Nomex fiber paper with a DLE-CVD process at 180 ^{o}C for 30 minutes. Then the CuMn alloy film was deposited at 220 ^{o}C for 30 minutes by the DLE-CVD copper process discussed in Chapter 2.

To deposit manganese nitride and CuMn alloy film on the Kevlar fibers, the Kelvar fibers were held by two clamps, which hang above the sample holder as shown in Fig. 5.1. A piece of silicon wafer was put under the kevlar fibers as a witness sample.

Figure 5.1. The sample holder set for Cu-Mn DLE CVD process of Kevlar Fibers

Manganese nitride was deposited on the Kevlar fiber as an adhesion layer at 180 ^{o}C for 10 minutes using the DLE-CVD process. Since the Kevlar fiber is hanging in the reactor space, it needed a higher reactor temperature to reach the same temperature as flat surfaces normally coated in this reactor.

In the DLE-CVD process for CuMn alloy, the reactor was held at a temperature of 220 ^{o}C for 40 minutes. CuMn alloy film was deposited on the MnN_x coated Kevlar paper and Kevlar fibers by the DLE-CVD process. In the DLE-CVD CuMn alloy process, the manganese precursor solution was injected into the evaporator at 6 g/hr and then the manganese precursor vapor in nitrogen gas was mixed with copper precursor vapor just prior to entering the deposition zone. A post-deposition anneal step at 350 ^{o}C for one hour in a nitrogen atmosphere was introduced if manganese was co-deposited with copper to diffuse the manganese from the copper-manganese alloy to the copper/fiber interface.

As a control experiment, the CuMn alloy film was deposited on Kevlar fiber directly without any manganese nitride barrier and adhesion layer by DLE-CVD process.

The conformality of manganese nitride and the copper-manganese alloy were evaluated by scanning electron microscopy (SEM). The cross section of the Kevlar coated by copper and manganese nitride was prepared by Focus Ion Beam (FIB) and the conductivity of fibers were evaluated by a Keysight E4980A electrical meter. The mechanical resistance of the conductive fibers was tested by our home-made test system.

5.3 Results and Discussion

DLE-CVD of MnNx and CuMn alloy film on Nomex fiber sheet paper

A conformal layer manganese nitride film can be prepared by DLE-CVD at 180 ^{o}C on the Nomex fiber sheet paper. A thick (around 100 nm) MnN_x layer on the Nomex fiber sheet paper is shown in Figure 5.2.

A smooth and continuous copper film was deposited on Nomex fiber paper by the DLE-CVD process at 200 ^{o}C for 30 minutes as shown in Figure 5.2.

Fig 5.2. (Left) MnNx on the Nomex fiber sheet. (Right) Cu and MnNx on the Nomex fiber sheet

The copper electrical sheet resistance is similar on the Nomex cloth (0.50 Ω/sq) and on a witness glass plate (0.48 Ω/sq), demonstrating that the film initiates and grows well on the polymer. The metal film survived a tape test, indicating that MnN_x can be a strong adhesion layer between copper and Nomex.

The cross-section image of copper and MnNx-covered Nomex fiber sheet paper is obtained by cutting the sample using sisscors before loading into the SEM analysis chamber, providing us with the cross-sectional image as shown in Figure 5.3. From the SEM image we can see that the fiber is fully covered by a layer of smooth copper film. The bottom of fiber is also covered by Cu because of the high penetration rate of DLE-CVD copper process.

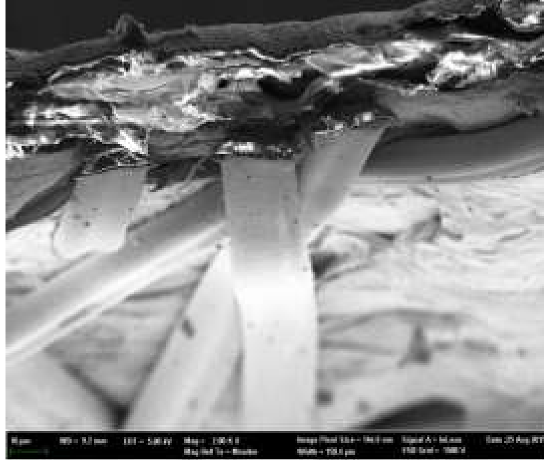


Figure 5.3. The cross section of copper and MnNx covered Nomex fiber sheet paper

DLE-CVD of MnNx and CuMn alloy film on Nomex fiber sheet paper

The same coating process was applied to Kevlar fibers with a diameter of 11 microns as shown in Fig 5.4.

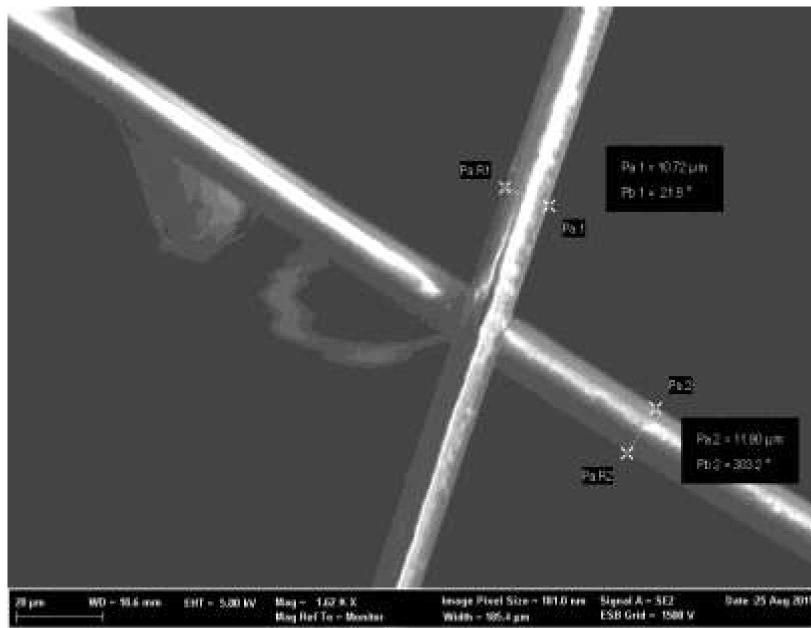


Fig 5.4. The Kevlar fiber SEM image

The Kevlar fiber was coated by MnN_x film using the DLE-CVD process at 180 ^oC for 10 minutes, after which copper-manganese film was deposited using the DLE-CVD process at 220 ^oC for 1 hour.

Fig 5.5 shows an SEM image of a copper-manganese and MnNx coated Kevlar fiber after cutting with FIB. A smooth, continuous layer of CuMn alloy film was deposited on the Kevlar fibers using the DLE-CVD process. The survival of the sample after FIB milling also shows the strong adhesion between the MnNx film and the Kevlar.

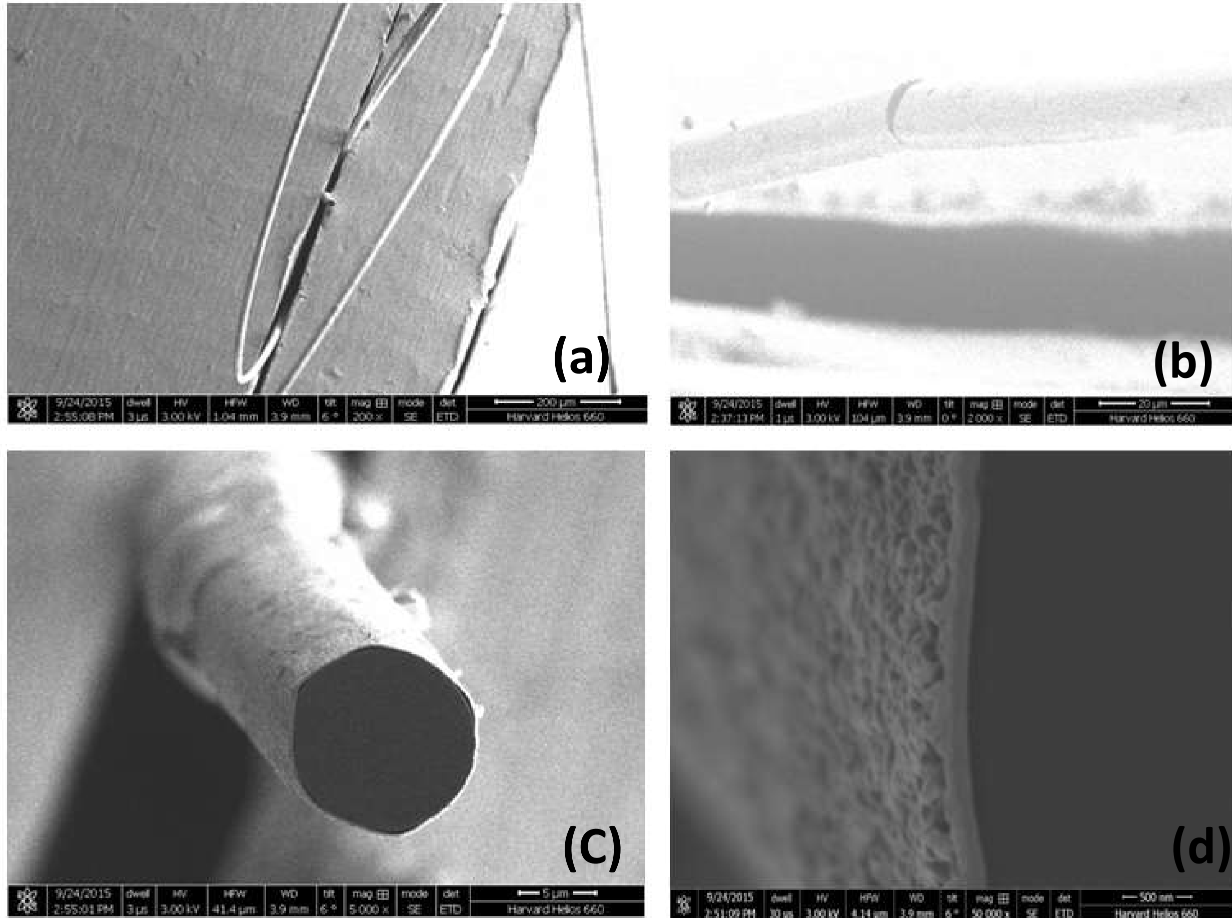


Fig. 5.5 a) The Cu-Mn alloy covered Kevlar fiber is bended and fixed on the FIB sample holder

b) The FIB milling process to get the cross-section Cu-Mn alloy coated Kevlar fibers

c) The Cross Section of Cu-Mn alloy coated Kevlar fibers

d) The interface of Cu-Mn alloy film and Kevlar fibers

Cu-Mn alloy film was also successfully coated on Kevlar fibers without the use of a MnN_x adhesion layer. The cross-section of the sample was prepared by FIB milling process. Fig. 5.6 a) shows a smooth and continuous Cu-Mn alloy film was achieved by DLE-CVD on Kevlar fibers even without an adhesion layer. Fig 5.6 b) shows that the interface between Cu-Mn alloy and Kevlar fibers is quite tight. Also the sample survival after the FIB milling process implies strong

adhesion. The reason why Cu-Mn film has good adhesion with Kevlar fiber is still an open question, one of the possibilities is because the bond between Cu, Mn atoms with O, N in the Kevlar fibers as shown in Fig 5.7.

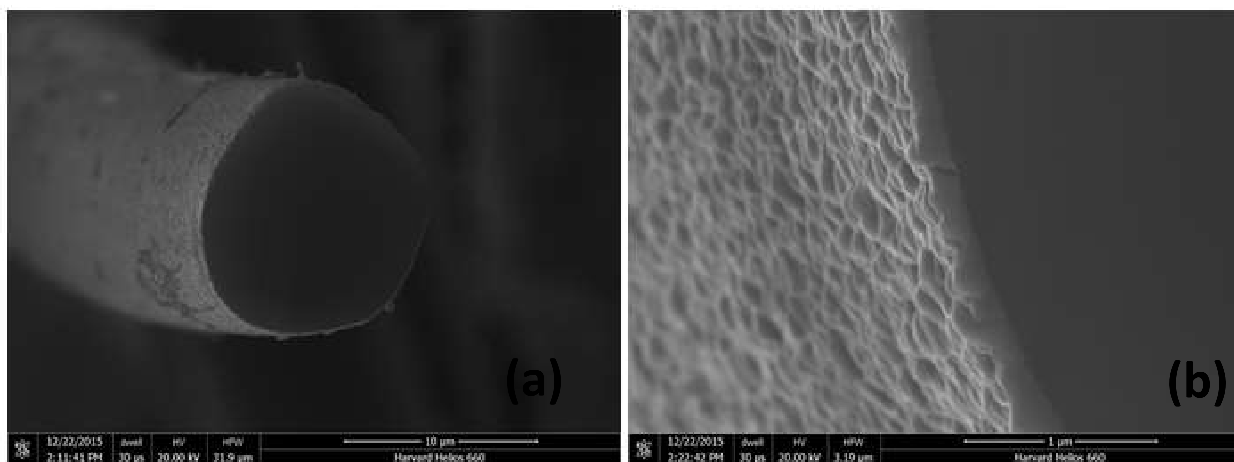


Fig 5.6 a) The cross section of Cu-Mn Alloy covered Kevlar (without MnNx)

b)The interface of Cu-Mn Alloy film and Kevalr (without MnNx)

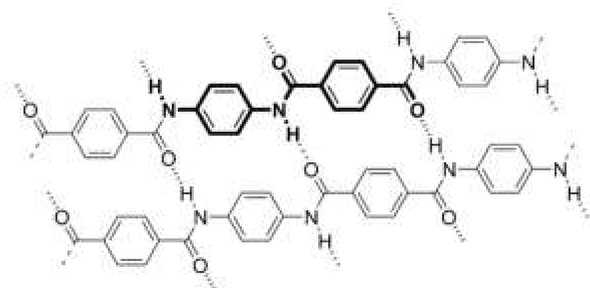


Fig 5.7. The molecular structure of Kevlar fibers

Electrical Characterization of Kevlar fibers covered by DLE-CVD Cu-Mn alloy film

Fig 5.8. Kevlar fibers coated with ~150 nm Cu-Mn alloy film

Sigma-Aldrich silver paste DGP80 was used as the electrode in the electrical characterization of the Cu-Mn alloy-coated Kevlar fibers. The DC resistance of as-deposited CVD Cu-Mn coated Kevlar Fiber with 1.5 cm long is 0.863 Ω. After 50 nm layer of ALD alumina-doped silica was deposited, the fiber became electrically insulating.

Mechanical Resistance Measurement

In order to assess the flexibility and electrical-mechanical endurance of CuMn alloy-coated Kevlar fiber, a simple home-made device as in Fig 5.9 was constructed to periodically bend the fiber and measure its resistance at the same time. We connected a fixed electrode and a moving electrode (robotic arm) with a 1.5cm Cu-coated Kevlar fiber (~150 nm Cu coating), and measured 0.863 Ohm DC resistance between the two electrodes. Then a motorized reciprocating motion was started at a frequency of 0.5 Hz, in which the maximum and minimum spacing between the two electrodes are 1.0 cm and 0.5 cm, respectively. After 0.5 million

bends, the resistance gradually increased to 0.867 Ohm, indicating that the tested Cu-coated Kevlar fiber has very high durability and is capable of maintaining its electrical conductivity after repeated bending.

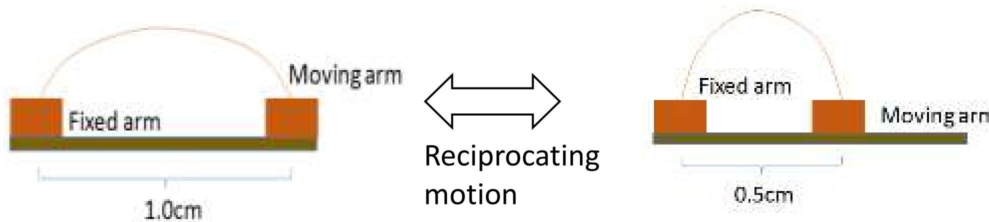


Figure 5.9. Home Made Mechanical Resistance Measurement System

5.4 Conclusions

Conformal and conductive copper-manganese layers for metallization of polyaramids were successfully prepared on Nomex fiber sheet paper and Kevlar fibers using the DLE-CVD process. An ALD layer of aluminum-doped silicon dioxide was then applied at a substrate temperature of about 250 ^{o}C to provide electrical insulation to the wires. The DLE-CVD copper-manganese film coated 11 μm diameter Kevlar fibers uniformly and conformably either with or without a MnN_x adhesion layer according to the cross section sample made by FIB process. The mechanical resistance of copper-manganese film coated Kevlar was tested through a robotic arm system, which shows after bending to a radius of 5 mm and then straightening more than half a million times the electrical resistance of the wire, was unchanged.

This process forms a highly robust and conductive copper-manganese alloy layers on the polyaramids fibers, which provide interconnects with high strength, flexibility, thermal stability and light-weight for connecting wearable systems.

Reference

[55] S. Armini, Z. El-Mekki, K. Vandersmissen, H. Philipsen, S. Rodet, M. Honore, a. Radisic, Y. Civale, E. Beyne, and L. Leunissen, "Void-Free Filling of HAR TSVs Using a Wet Alkaline Cu Seed on CVD Co as a Replacement for PVD Cu Seed," *J. Electrochem. Soc.*, vol. 158, no. 2, p. H160, 2011.

[56] J. K. Vrtis and D. Ph, "Enabling Smart Wearable Technology : Flexible , Stretchable Interconnect," 2014.

[57] R. G. Gordon and J. Feng, "Vapor Deposition of Copper-Manganese Interconnects," pp. 2–4.

[58] R.Paraskov;, E.Becker;, T.Riedl;, H.Johannes;, and W.Kowalsky, "Large Area Elcetronics Using Printing Methods," *Proc. IEEE*, vol. 93, no. 7, pp. 1321–1329, 2005.

[59] J. Li, T. Monaghan, S. Masurtschak, A. Bournias-Varotsis, R. J. Friel, and R. A. Harris, "Exploring the mechanical strength of additively manufactured metal structures with embedded electrical materials," *Mater. Sci. Eng. A*, vol. 639, pp. 474–481, 2015.

[60] L. Hu, M. Pasta, F. La Mantia, L. Cui, S. Jeong, H. D. Deshazer, J. W. Choi, S. M. Han, and Y. Cui, "Stretchable, porous, and conductive energy textiles," *Nano Lett.*, vol. 10, no. 2, pp. 708–714, 2010.

[61] Du Pont, "Kevlar Technical Guide." pp. 1–32, 2012.