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# InAlN/GaN MOSHEMTs with High Drain Current of 2.3 A/mm High On/Off Ratio of $10^{12}$ and Low SS of 64 mV/dec Enabled by Atomic-Layer-Epitaxial MgCaO as Gate Dielectric

Hong Zhou<sup>1</sup>, Xiabing Lou<sup>2</sup>, Heng Wu<sup>1</sup>, Sami Alghamdi<sup>1</sup>, Shiping Guo<sup>3</sup>, R. G. Gordon<sup>2</sup>, and Peide D. Ye<sup>1\*</sup>

<sup>1)</sup> School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906, U.S.A

<sup>2)</sup> Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.

<sup>3)</sup> IQE RF LLC, Somerset, NJ 08873, U.S.A.

\* Tel: 1-765-494-7611, Fax: 1-765-496-6443, Email: [yep@purdue.edu](mailto:yep@purdue.edu)

Recently, GaN-based high-electron-mobility-transistor (HEMT) has demonstrated its promise in high frequency [1], high power [2] and low noise [3] electronic devices. The lattice matched InAlN/GaN HEMT structure provides a higher 2D electron density than AlGaN/GaN due to a larger bandgap offset and minimized short-channel-effects due to its thinner barrier. However, because of its several-nm thin barrier, those devices usually suffer from high gate leakage and interface trap issues, the device off-state performance is degraded and thereby the off-state breakdown voltage is decreased. Therefore, finding a good method to reduce the gate leakage and interface trap density is of great importance to improve the device off-state performance. In this study, we use atomic layer epitaxial MgCaO as gate dielectric to fabricate sub-100nm InAlN/GaN MOSHEMTs with significantly improved maximum drain current, current on/off ratio and low subthreshold swing.

Fig. 1 shows the device structures of the InAlN/GaN HEMT and MOSHEMT, respectively. Device fabrication was started with mesa isolation by  $\text{Cl}_2/\text{BCl}_3$  etching. Ohmic contacts were formed by depositing Ti/Al/Au (15/60/50 nm) followed by  $775^\circ\text{C}$  rapid thermal annealing in  $\text{N}_2$  with optimized  $R_c$  of  $0.3 \Omega\cdot\text{mm}$ . Two splits of experiments are performed. 1) Device set A was treated by  $\text{O}_2/\text{Ar}$  plasma with gas flow of 12/120 sccm at the power of 100 W for 5 minutes. These devices are used as reference ones that shows the importance of surface passivation [4]. 2) Device set B was first deposited by 4nm of atomic-layer epitaxial (ALE) MgCaO, followed by 2nm  $\text{Al}_2\text{O}_3$  as a capping layer. Single crystalline MgCaO offers the right band offset and the best interface on AlInN/GaN system.[5] This is the central point of this work. Finally, the gate was formed by Ni deposition followed with a lift-off process. The devices that have  $L_g=85$  nm and  $L_{sd}=1 \mu\text{m}$  are used as the representative ones in this abstract. All the lithography processes were carried out using a Vistec VB6 electron beam lithography system.

Fig 2 (a) and (b) show the DC output characteristics ( $I_d$ - $V_d$ ) of the  $\text{O}_2$  plasma treated InAlN/GaN HEMT and the InAlN/GaN MOSHEMT with ALE MgCaO as gate dielectric. Thanks to the 6 nm thick gate oxide, a high gate bias of 4 V is applied and the  $I_{ds,max}$  has reached 2.3 A/mm with an on-resistance ( $R_{on}$ ) of  $1.2 \Omega\cdot\text{mm}$ . The  $I_{ds,max}$  is significantly improved, compared to 1.7 A/mm for HEMT, due to the capability of further positive bias the gate voltage and dielectric passivation of source and drain regions of the InAlN surface. Despite the thicker gate to channel spacing (14 nm) compared to HEMT, MOSHEMT still exhibits a high transconductance of 465 mS/mm at  $V_{ds}=5$  V (shown in Fig.3 (a)). Fig. 3 (b) depicts the log-scale  $I_d$ - $V_g$  curves of the MOSHEMT and HEMT; respectively. The MOSHEMT demonstrates one of the highest on/off ratio of  $10^{12}$ . The higher on/off ratio of the MOSHEMT (compared to HEMT of  $10^8$ ) is from the much lower gate leakage current exhibited by the MOSHEMT. Thanks to the stable process, more than 80% of those devices on the same chip show an on/off ratio of  $10^{10}\sim 10^{12}$  with  $L_g$  from 250 to 80 nm. Fig. 3 (c) describes the zoom-in image of the  $I_d$ - $V_g$  of the MOSHEMT in the subthreshold region. The SS of the  $V_{ds}=0.05$  V,  $V_{ds}=2.5$  V,  $V_{ds}=5$  V are quite similar with small value of 64 mV/dec. This low SS indicates the good interface between the ALE MgCaO and InAlN barrier. It suggests that the lattice matched epitaxial MgCaO on the InAlN barrier is the main reason for these good on-state and off-state device performances.

In conclusion, high performance sub-100 nm gate length InAlN/GaN MOSHEMTs are demonstrated using lattice matched ALE MgCaO as gate dielectric. The representative MOSHEMT has an  $I_{ds,max}$  of 2.3 A/mm,  $R_{on}$  of  $1.2 \Omega\cdot\text{mm}$ , SS of 64 mV/dec, and a high on/off ratio of  $10^{12}$ . ALD MgCaO shows the promise for GaN MOS technology. The work at Harvard University and Purdue University is supported by ONR and AFOSR, respectively.

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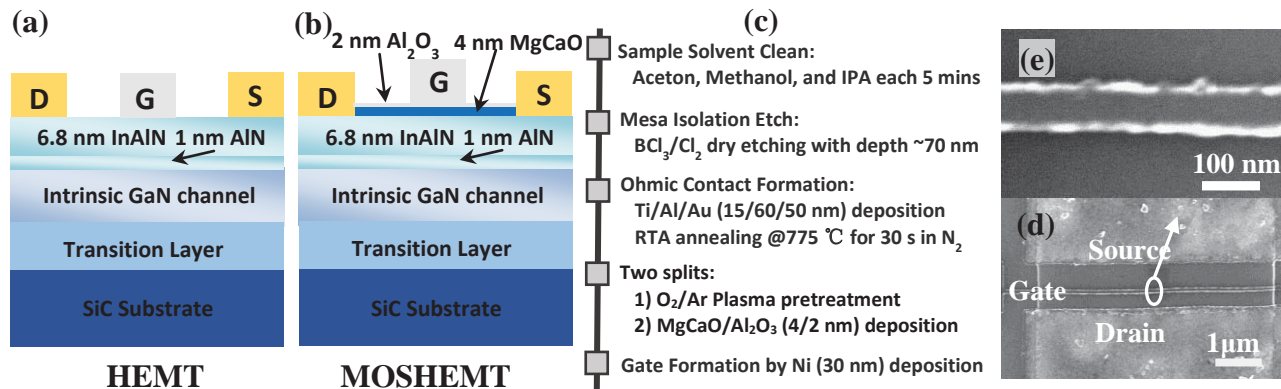


Fig. 1 Schematic of (a) GaN HEMT (left), (b) MOSHEMT (right), (c) the detailed two splits of devices fabrication steps, (d) overview of the fabricated device with source, drain and gate as shown, (e) zoom-in view of the device with  $L_g=85\text{nm}$ .

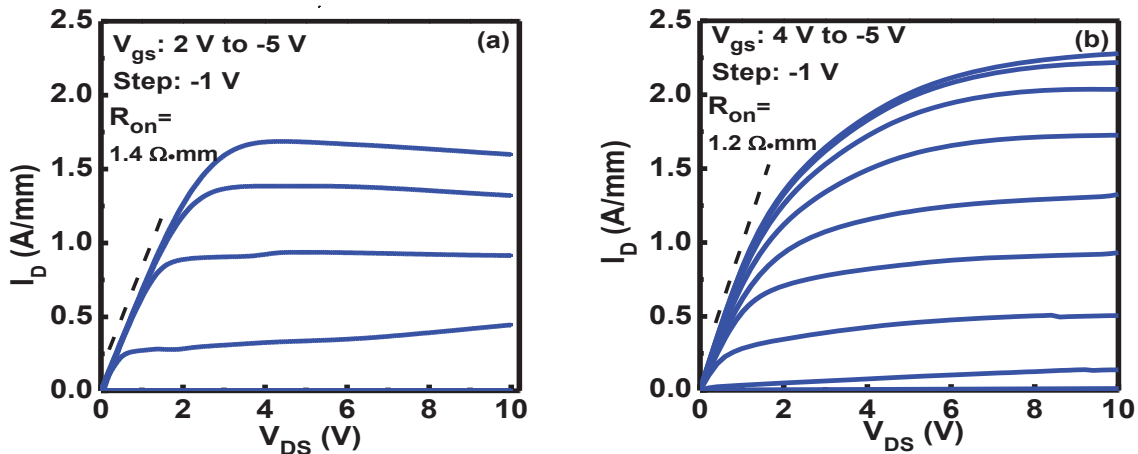


Fig. 2 (a) Output characteristics of an O<sub>2</sub>/Ar pretreated GaN HEMT with an  $I_{ds\text{max}}=1.7 \text{ A/mm}$ , on-resistance  $R_{on}=1.4 \Omega \cdot \text{mm}$ ,  $V_T=-1.75 \text{ V}$ , and  $g_{m\text{max}}=600 \text{ mS/mm}$  at  $V_{ds}=4 \text{ V}$ . (b) Output characteristics of a GaN MOSHEMT with ALE MgCaO as gate dielectric. This device demonstrates an  $I_{ds\text{max}}$  of 2.3 A/mm and  $R_{on}=1.2 \Omega \cdot \text{mm}$ .

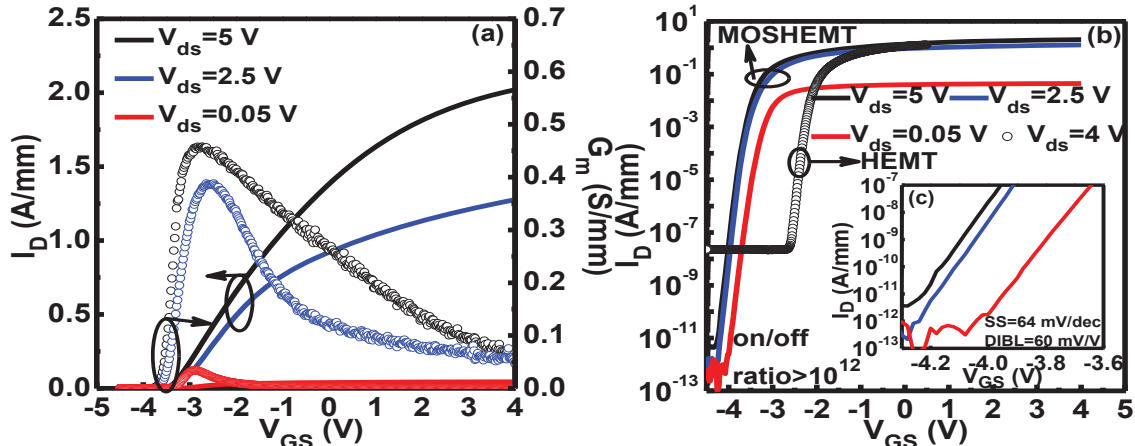


Fig. 3 (a)  $I_d$ - $V_g$  transfer characteristics of MOSHEMT for  $V_{ds}=5 \text{ V}$ ,  $V_{ds}=2.5 \text{ V}$ , and  $V_{ds}=0.05 \text{ V}$ ; respectively. A high transconductance of 465 mS/mm is obtained with  $V_T=-3.51 \text{ V}$  at  $V_{ds}=5 \text{ V}$ . (b) Log-scale view of the  $I_d$ - $V_g$  for both HEMT and MOSHEMT. A high on/off ratio  $>10^{12}$  and  $10^8$  are obtained for MOSHEMT and HEMT, respectively. Fig. 3(c) as the inset in Fig.3 (b) shows the zoom-in view of  $I_d$ - $V_g$  (for MOSHEMT) in the subthreshold region. Similar SS of 64 mV/dec is observed for  $V_{ds}=5 \text{ V}$ ,  $V_{ds}=2.5 \text{ V}$ , and  $V_{ds}=0.05 \text{ V}$  with a small DIBL=60 mV/V determined from  $V_{ds}=0.05 \text{ V}$  (red) and  $V_{ds}=2.5 \text{ V}$  (blue) curves.