Advanced Metallization Processes for Complex Structures in Microelectronics by Direct-Liquid-Evaporation Chemical Vapor Deposition

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Advanced Metallization Processes for Complex Structures in Microelectronics by Direct-Liquid-Evaporation Chemical Vapor Deposition

A dissertation presented

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Abstract

With the rapid advancement of semiconductor industry, fabrications of complex

microelectronic devices are going beyond the conventional planar geometries into

three-dimensionality (3D). Besides, since the emerging of flexible and wearable

consumer electronics, it is also desired to break the limitation of conventional rigid

electronic devices and transform toward flexible devices. In order to provide

fundamental frameworks for 3D electronics and flexible electronics, strategies to create

complex structures at nano-/micro-scales, including interconnect architectures, need to

be developed. For nano-scale high-aspect-ratio metal interconnects, great challenges

are yet to be overcome because of the rigorous requirements of high-precision

fabrication, high metal uniformity and conformality, as well as special liner and capping

layers. Promising solutions to these challenges are offered by direct-liquid-evaporation

chemical vapor deposition (DLE-CVD) technique developed in recent years. DLE-CVD is

able to quantitatively deliver high-throughput precursor into deposition chambers with

high controllability and vaporization efficiency, which provides high-quality metallization

layers even deep inside complex structures, or on flexible polymer substrates.

     In this thesis, advanced metallization processes based on DLE-CVD are described.

The deposited metallic materials from these processes, including cobalt (Co), nickel (Ni),

nickel silicide (NiSi) and copper (Cu), are thoroughly characterized and studied by electron microscopies, elemental analysis tools, atom probe tomography (APT), etc. Applications of these metallization processes in 3D electronics are demonstrated directly on high-aspect-ratio structures fabricated by reactive ion etching (RIE) technique. Furthermore, potential utilization of DLE-CVD processes to metallize the surface of polymer fibers, which can be used as flexible interconnects, is also discussed.

Chapter 1 provides a background introduction to the basics of metallization strategies and applications, and discusses potential applications of these strategies.

Chapter 2 describes detailed methods to fabricate well-defined high-aspect-ratio structures, and introduces an intriguing self-smoothing phenomenon observed in aluminum-catalyzed silicon dioxide (SiO_2) atomic layer deposition (ALD), which can be used to create smooth-wall trench structures with ultrahigh aspect ratios up to 100:1.

Chapter 3 presents in-detail study of DLE-CVD cobalt (Co), in which the deposition process of highly conformal, pure, and smooth nanocrystalline Co metal films is described. All-around encapsulation of nano-scale copper (Cu) interconnect by DLE-CVD Co is demonstrated to be an effective strategy to enhance interconnect reliability, stability, and operation life.

In chapter 4, APT technique is used to study our metallic materials deposited by DLE-CVD. Compositional and structural information are acquired with atomic resolution.

And chapter 5 explores the potential application of DLE-CVD Co as the initial metallization layer on polymer fibers, to create conductive flexible interconnects.

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Jun Feng
Cambridge, Massachusetts
June 22, 2017

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Chapter 1   Introduction

1.1   Metallization Processes in Modern Microelectronics

1.1.1   The Role of Metallic Materials in Microelectronics

As modern semiconductor devices scale toward the sub-10-nm regime, advanced

microelectronic processes require highly efficient integration of multiple functioning

parts, including semiconductor channels, insulating layers and metal interconnects.[1-2] In

complex microelectronic architectures, active components (transistors, memory cells,

sensors, etc) are usually at nano-scale sizes. However, practical applications of these

components require intermediate "bridges" to enable access to the small units by

larger-scale interfaces. Therefore, multiple layers of interconnects, from the smallest

local interconnects to the largest global interconnects, are needed in semiconductor

devices. Moreover, since more and more active components are being integrated into

smaller areas, it is becoming increasingly challenging to fabricate the "roads" to enable

communications among individual functioning units in the extremely complex

microelectronic architectures.[3-4] In this regard, metallic material materials that can

efficiently conduct electrons are required, for both the "bridges" to grant vertical

accessibility and the "roads" to provide lateral interactions among units, as

schematically illustrated in Figure 1.1.

Since IBM and Intel first introduced the replacement of aluminum with copper for

microelectronic interconnects, tremendous efforts have been put on the developments

of copper metallization processes.[5] The lower electric resistivity of copper (16 nOhm·m)

compared with that of aluminum (28 nOhm·m) makes it possible to achieve faster, smaller and denser microprocessors, because less material is needed for interconnects transporting the same amount of electric current, thus improving the overall efficiency.[6] However, the introduction of copper into microelectronic devices also brought many new challenges, especially the issues caused by the high migration and diffusion rates of copper atoms.[7]
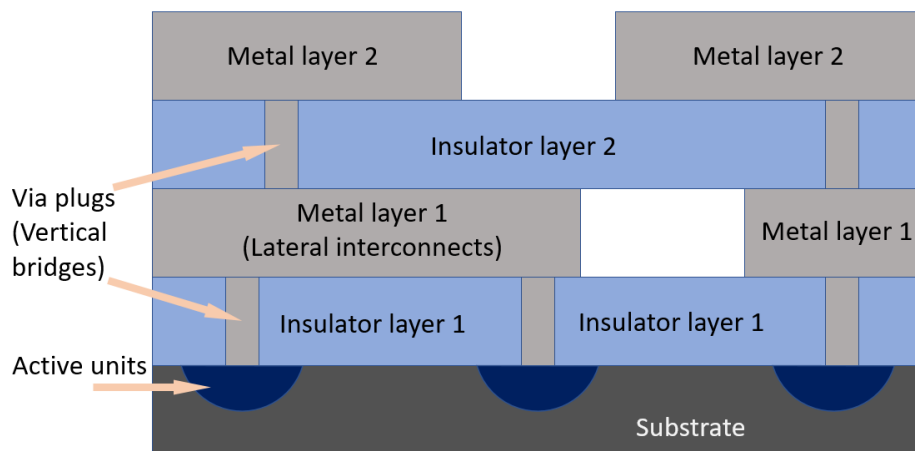
Figure 1.1. Illustration of the functions of different layers of metal interconnects

To overcome this issue, it is important to effectively separate or block copper atoms away from any diffusion-sensitive areas.[8] Tantalum (Ta) and tantalum nitride (TaN) have been widely used in modern microelectronic systems as diffusion barriers to prevent copper atoms from penetrating into dielectric layers or semiconductor channels.[9] Many other metallic nitride materials including titanium nitride (TiN), tungsten nitride (WN),

manganese nitride (MnN_x), and cobalt nitride (CoN_x) are also being developed as copper

barriers for better semiconductor device life time and reliability.[10-12]

Another challenge for copper interconnect technology is that copper does not form

Ohmic contact with silicon, which is due to the misalignment between the work function

of copper and the fermi level of silicon.[13] Thus, intermediate metallic materials are

needed to connect silicon semiconductor devices with upper-level copper interconnects.

Metal silicides, including nickel silicide (NiSi), cobalt silicide ($CoSi_2$), titanium silicide

($TiSi_2$) and platinum silicide (PtSi), are introduced between metal interconnects and

active semiconductor contact areas.[14] For example, in order to form ohmic contact to

silicon, titanium silicide can be formed at the silicon surface by depositing a thin layer of

titanium metal onto the contact area, followed by 700~850 °C annealing.[15] However, it

remains a challenge to controllably form high-quality, low-resistance, and conformal

silicide at lower temperatures that are compatible with current semiconductor

manufacturing processes.

For the connection between silicide contacts and vias, tungsten (W) plug processes

have been developed in current technologies for both front-end and back-end

metallization processes as the metal filling.[16] At the 14 nm technology node and beyond,

the critical dimension (CD) of contact is less than 25 nm, and could only incorporate

about 3 nm of tungsten metal as the plug material.[17] However, tungsten plug filling

requires a wetting layer for better nucleation because tungsten does not nucleate well

on silicon surfaces.[18] With only a few nanometers of tungsten, it is a great challenge to

form uniform and continuous thin film material for plugs. Also, the conductivity of tungsten dramatically increases as the size shrinks due to surface scattering of electrons.[19] Therefore, cobalt thin film processes have been developed recently to replace tungsten, since cobalt does not require special wetting layer to form continuous film on silicon-based surfaces, and has higher conductivity when fabricated into ultra-small interconnects.[20]

Beyond the plug materials, intermediate and global interconnects are mostly micrometer-scale copper metal wires encapsulated by barrier and liner layers.[21] In modern microelectronic system, these larger interconnects form extremely complicated three-dimensional (3D) architecture and require highly conformal coating of metal materials into high-aspect-ratio structures.[22] Of note, gas phase metal coating techniques usually have low deposition rates, thus giving unfavorably low productivity. To increase efficiency, it is a common strategy to utilize a vacuum-deposited metal thin film as seed layer, then use electroplating to fill up the interconnects.[23] Therefore, it is crucial to develop highly conformal metal seed layer deposition processes to enable electroplating on complex 3D interconnect architectures. Besides, the design and fabrication of vertical metal interconnects also requires proper insulating and barrier layers, which are also parts of the great challenges for the advancement for copper interconnect systems.

Overall, metallic materials are crucial parts for semiconductor devices, which enable the access and utilization of ultra-small active units, and comprise the complex

electronic communication architectures within the devices. In the past decades, although substantial advancements have been achieved with copper interconnect technology, challenges remain for the realization of better-performance, higher-density, and higher-efficiency electronic devices in the future.

1.1.2 Vapor Deposition Methods for Metallic Materials

Metallic materials can be deposited from vapor by either physical methods or chemical methods. In physical vapor deposition (PVD) methods, materials are directly vaporized by heat (thermal evaporation), laser (pulsed layer deposition), electron beam (e-beam evaporation), or ion/plasma bombardment (sputtering), and then re-condense onto the sample substrates.[24] Since PVD methods directly take out materials from a metal target source and deposit them into thin films, the chemical composition of deposited film can be usually guaranteed by the purity of target sources, and the deposition rate can also be readily controlled by the intensity of excitation (temperature, e-beam current, laser intensity, etc.).[25] In this regard, PVD offers high controllability and good reproducibility, as well as high deposition rates, which are all very favorable for production-level industrial applications. However, for those applications that need to use uncommon materials, it may be difficult and cost-ineffective to make the target source for PVD processes. Moreover, PVD processes are not capable of conformal coating, which substantially limits their applications when it comes to the coating of complex structures.[26]

On the other hand, chemical vapor deposition (CVD) is a coating technique by inducing chemical reactions on sample surfaces to form desired materials. Unlike PVD processes, which only use one source material, CVD processes usually involve two or more source materials called precursors.[27] For example, tungsten nitride (WN) can be deposited by introducing gas-phase tungsten fluoride (WF_6) and ammonia (NH_3) together into deposition chamber at the same time.[28] By proper process development, the chemical deposition reactions can be set to only take place on sample surfaces to produce thin films, rather than to produce powders with gas-phase reactions.[29] Since CVD processes are surface-dependent, this technique can produce highly conformal coatings even in very high-aspect-ratio structures, which can hardly be achieved with conventional PVD methods.[30] Figure 1.2 shows the difference in the coating characteristics between PVD and CVD processes. Also, for those materials that are difficult to be made into PVD targets, CVD is also a practical alternative. Generally, CVD offers highly conformal and uniform coatings of a large variety of chemical compounds, which is highly favorable for the manufacturing of modern 3D microelectronic systems.[31] However, CVD processes usually have lower deposition rates, higher process temperature, and sometimes lower-purity thin films compared with PVD methods. Therefore, there are still many challenges in the development of advanced CVD processes for practical industrial applications.
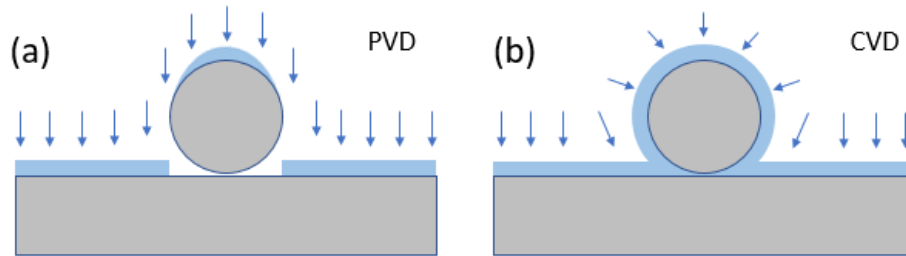
Figure 1.2. Difference between the deposition characteristics of (a) PVD and (b) CVD.

1.1.3 Thin Film Deposition in High-Aspect-Ratio Structures

As discussed in previous context, CVD processes offer the feasibility of depositing thin films into complex structures. Nevertheless, proper designing of CVD processes is still required to realize the coating of structures with super-high aspect ratios.[32]
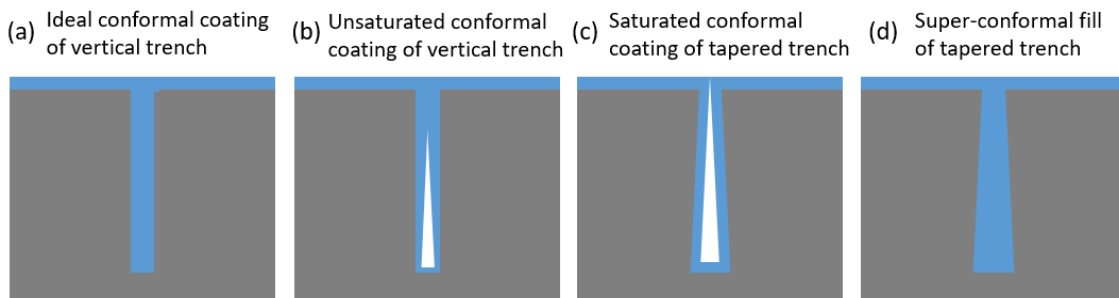
Figure 1.3. Different filling behaviors with different conformal coating processes. (a) Ideal fill of an ideally vertical trench; (b) Partial fill of a vertical trench by unsaturated conformal deposition process, leaving a void in the trench; (c) Partial fill of a tapered trench with sloped side walls by saturated conformal deposition process, leaving a void in the trench; (d) Complete super-fill of a trench with sloped side walls by super-conformal deposition process.

Microscopically, conformal coating can be achieved on nonplanar substrates either when the adsorbed precursor molecules can diffuse laterally on sample surfaces, or when the precursors have low sticking coefficients and tend to re-emit into the gas phase.[33-34] The prerequisite for conformal coating by either mechanism is that precursor molecules need to physically diffuse deep into any complex structures, e.g. holes or trenches. When the precursor concentration is not high enough to saturate all sample surface, step coverage will gradually decrease as the aspect ratio increases, thus causing a tapered deposition profile, which we here define as an unsaturated region as shown in Figure 1.3(b) and Figure 1.4(b).[35]
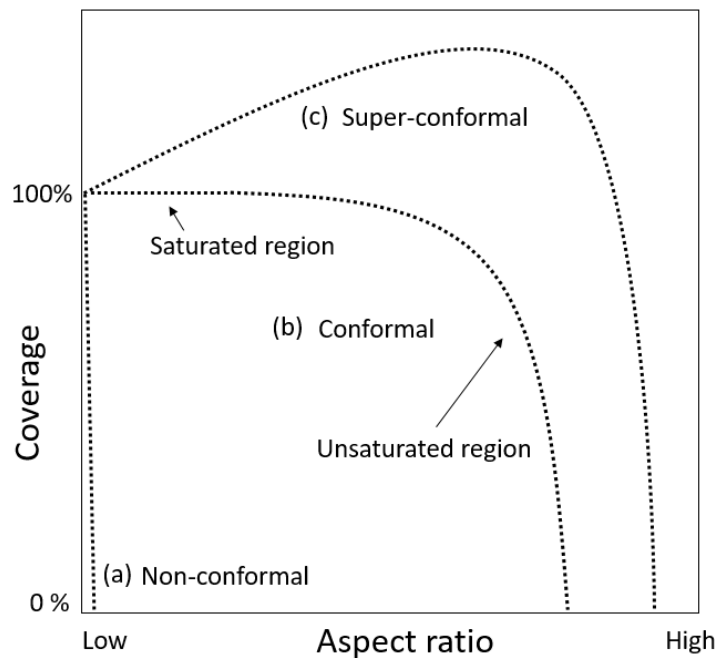
Figure 1.4. Illustration of different step coverage behaviors of non-conformal, conformal, and super-conformal thin film deposition processes.

Practically, it is highly challenging to fully saturate entire sample surfaces and create identical thickness at all aspect ratios. Therefore, super-conformal deposition processes (as depicted in Figure 1.3d and Figure 1.4c) were developed in recent years to achieve complete fills of trench or hole structures. There are generally two strategies for super-conformal coating: 1. Introducing a catalyst that can accelerate deposition rate at the bottom of a trench;[36] 2. Special designing and utilizing the diffusivity difference of co-reactants to kinetically increase growth rate at the deeper parts of a trench or hole.[32]
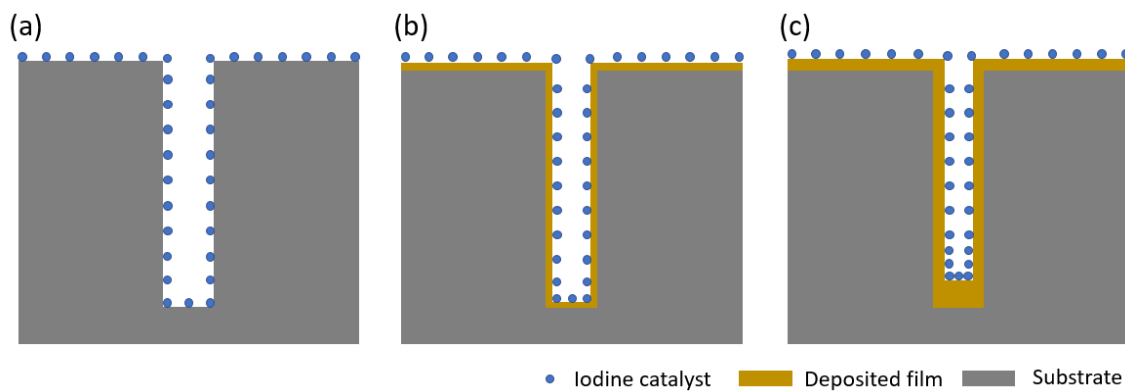
Figure 1.5. Illustration of iodine catalyzed bottom-up super-conformal coating on a trench. (a) Trench with iodine catalyst conformally absorbed on the side walls; (b) Initial growth rate is consistent throughout the trench; (c) As the film grows, iodine concentration increases at the bottom, thus increasing the growth rate at the bottom.

With the catalyst method, a special chemical needs to be introduced into the deposition chamber prior to the deposition process. For example, ethyl iodine can

catalyze the Cu and Mn CVD processes with amidinate precursors.[11] As shown in Figure 1.5, iodine concentration keeps increasing at the bottom of the trench as the deposition continues, thus further increasing the growth rate at the bottom of high-aspect-ratio structures.

With regard to the kinetic designing method for the implementation of super-conformal coating, no additional chemical need to be introduced into the deposition process. However, this method has very specific requirements for the selection of precursors. For example, super-conformal MgO growth can be realized with Mg(DMADB)$_2$ and H$_2$O precursor, because of their competitive adsorption behaviors on sample surfaces, as well as their difference in diffusivities, which are all hard requirements on the physical properties of the precursor, limiting its applications with wider variety of precursors for different purposes.[32]

Conformal and super-conformal thin film deposition techniques are highly important for future developments of advanced microelectronics, because higher-density package of semiconductor devices require the incorporation of functional materials onto three-dimensional frameworks with high aspect ratios.[37-38] However, currently developed conformal and super-conformal metal deposition processes are very limited. Many available processes either requires expensive apparatus or are unable to fulfill requirements (conformality, purity, deposition rate, etc.) for cutting-edge electronic devices manufacturing applications. Further scientific and technological developments in conformal coating techniques in complex structures are needed for the

design and fabrication of next-generation electronics. In chapter 2 of this thesis, a super-conformal self-smoothing Al-catalyzed SiO_2 ALD process is described, and used to fabricate smooth-wall trench structures with ultrahigh-aspect-ratio structures.

1.2   Direct-Liquid-Evaporation (DLE) CVD of Metallic Materials

1.2.1   Concepts and Advantages of DLE-CVD

Direct-liquid-evaporation chemical vapor deposition (DLE-CVD) is a CVD process with DLE precursor delivery system. In contrast to conventional CVD with bubbler sources of vapor, liquid precursor solutions in DLE-CVD systems are stored unheated and directly injected into the heated evaporation region.[39] The DLE process heats a precursor only very briefly, thereby avoiding decomposition that can occur when a conventional bubbler is heated for long time, decreasing unwanted carbon or organic contamination in the films. Moreover, the precursor delivery rate of DLE-CVD is controlled by the very stable injection rate of a liquid precursor or a precursor solution, instead of the variable precursor vapor pressure found in conventional bubblers.[40] These features of DLE-CVD enable formation of films with much higher conformality and better reproducibility than conventional CVD systems.

As illustrated in the diagram shown in Figure 1.6, precursor solution of DLE-CVD is stored outside of an oven, and delivered into the deposition chamber after evaporating in a heated vaporization loop. The precursor delivery rate is stably controlled and measured by a liquid mass flow-controller (MFC) immediately before it flows into the

vaporization loop. With this design, precursor delivery rates of DLE-CVD are not limited

by precursor vapor pressures like traditional CVD is. Therefore, precursors in a DLE-CVD

deposition chamber can reach much higher gas-phase concentrations and saturate all

surfaces in complex structures, minimizing the growth rates difference at positions with

different aspect-ratios.[41]
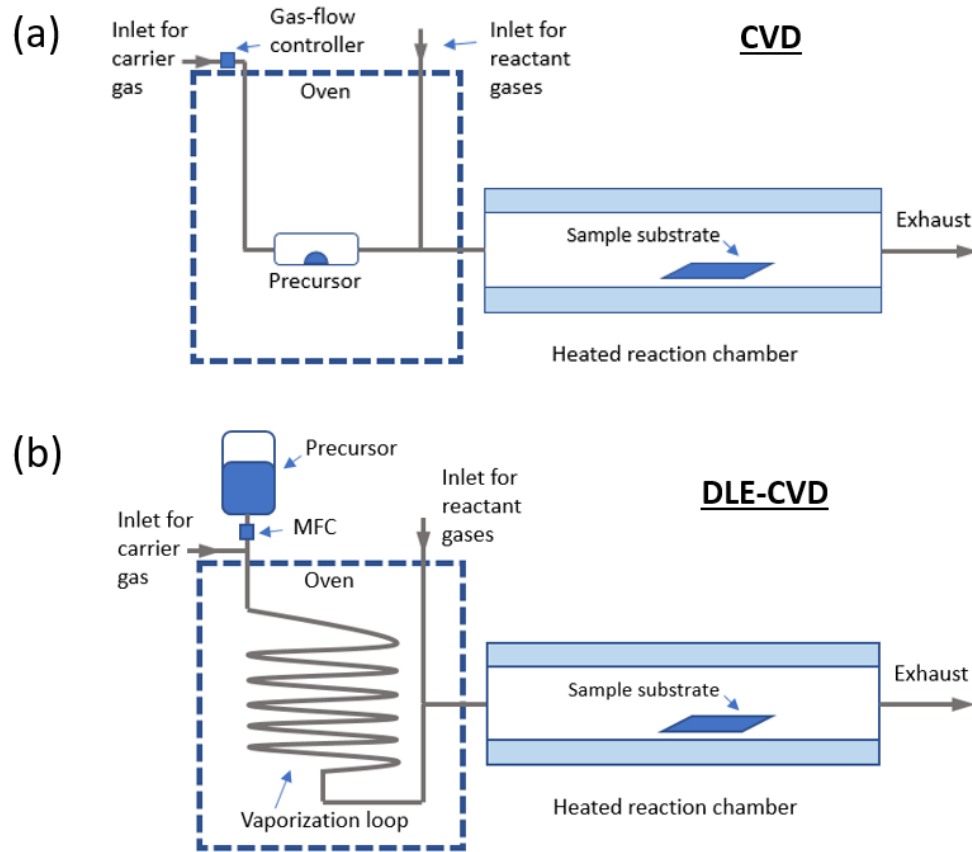
Figure 1.6. Diagrams showing the design difference between the precursor delivery

systems between (a) conventional CVD and (b) DLE-CVD system.

1.2.2 DLE-CVD Precursors and Processes for Metal Thin Films

In our previous works, four metal DLE-CVD processes have been developed with four different precursors, which are summarized in Figure 1.7. So far, all precursors used for our DLE-CVD depositions are metalorganic compounds with acetamidinate legends. At room temperature, these precursor compounds are all solids. Precursor solutions are made by dissolving solid-state precursors in inner organic solvents, like tetradecane and trihexylamine. These solvents are chosen because they have vapor pressure similar to the precursors, and does not decompose or interact with precursors or other co-reactants during the deposition processes.[42]

(a)

N,N'-(diisopropylacetamidinate) Cobalt(II)

(b)

N,N'-(ditertbutylacetamidinate) Nickel(II)

(c)

N,N'-(ditertbutylacetamidinate) Manganese(II)

(a)

N,N'-(diisobutylacetamidinate) Copper(I) dimer

Figure 1.7. Precursors used in our developed DLE-CVD processes.

For cobalt, nickel and copper metal depositions, we used tetradecane as the solvent and performed vaporization at 150 °C under vacuum of 5 to 30 Torr. Deposition chamber temperatures were set to be in the range 180 ~ 280 °C, while the actual sample holder is heated to be 5 ~ 15 °C higher than the chamber temperature by an embedded heater, in order to form thin films on sample surfaces rather than the chamber wall. Deposition pressure is controlled and maintained at 5 ~ 30 Torr by a butterfly valve, with continuous flows of carrier gas and co-reactant gases. Copper amidinate precursor has high reactivity directly with hydrogen, but nickel and copper amidinate precursors require the introduction of a certain amount of ammonia to deposit a metal film. The process for manganese metal deposition is mostly the same as that of copper, but with slightly higher chamber temperature (230 ~ 300 °C), indicating that the manganese amidinate precursor has slightly lower reactivity with hydrogen than the copper precursor.[43]

Overall, in order to develop DLE-CVD processes for different kinds of metal materials, proper designing and selection of solvent, vaporization temperature, substrate temperature, deposition pressure, and co-reactant gas flows are highly important. In chapter 3 of this thesis, detailed studies of Co DLE-CVD parameters and deposition characteristics will be discussed. Also, in chapter 4, atom probe tomography (APT) characterizations are used to study the thin films deposited by DLE-CVD processes at atomic resolution.

1.3   Surface Metallization of polymeric materials

1.3.1   Conductive Polymer Fibers and Flexible Electronics

While silicon-based electronics revolutionized information carriers by steering away from papers toward flat displays, it also sacrificed the mechanical flexibility and robustness of the traditional media.[44] In this regard, flexible electronics is emerging as a solution to bring back the advantageous features of paper materials.[45-46] In addition to the complex interconnecting architectures as silicon-based electronics requires, flexible electronics further demands high flexibility and mechanical strength of its interconnects.[47-49] Several potential strategies to fabricate flexible interconnects have been reported in recent years, including carbon nanotube yarns,[50] reduced graphene oxide fibers,[51] silver nanowire coatings,[52] conducting polymers,[53] and metallization of polymer fibers,[54] etc. Among these strategies, direct surface metallization of commercial polymer fibers offers the advantage of higher scaling-up feasibility, and better inheritance of the well-established mechanical performance of polymer cores.[55] Nevertheless, it remains a great challenge to develop efficient metallization methods for the formation of uniform and smooth all-around coatings on densely packed fiber yarns or threads.

1.3.2   Surface Metallization Methods for Polymeric Materials

To achieve high-quality surface metallization of insulating polymer fibers, extensive studies have been conducted on polymer surface processing and metal deposition techniques.[56-57] Of note, fibers are high-aspect-ratio structures morphologically, which brings the need of conformal coating methods, rather than traditional anisotropic deposition techniques like thermal evaporation and sputtering.[58] Electroless deposition and other solution deposition methods were widely used for metallization of insulating objects, but liquid-phase methods usually either require toxic chemical solutions or produce relatively weakly adhered metal/polymer interfaces, which is not favorable for industry-scale flexible electronic applications.[59]
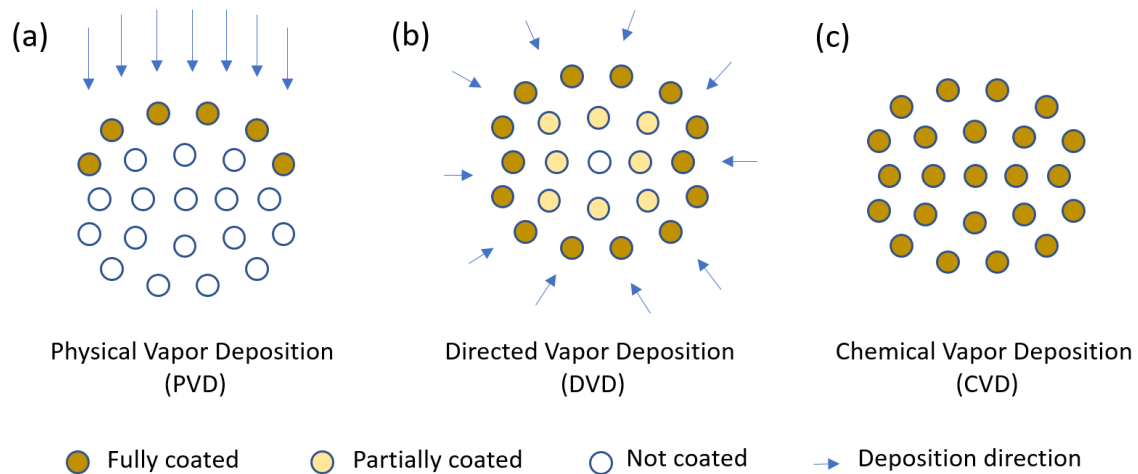

Figure 1.8. Deposition characteristics of PVD, DVD and CVD on a bundle of polymer fibers from a cross-section view.

Another commercialized coating method for fiber structures is directed vapor deposition (DVD), which can make near-conformal metal depositions onto thick fiber

(>100 um diameter) arrays with large fiber-to-fiber spacing (>1 mm).[60] Whereas for the metallization of smaller fibers with higher densities, i.e. higher aspect-ratios, DVD method still could not achieve satisfying results.[61] In this regard, chemical vapor deposition (CVD) of metal is a possible technique to accomplish the challenge of all-around coating of fibers, since it provides highly conformal and high-quality coatings even in very high-aspect-ratio structures.[62]

Figure 1.8 illustrates different gas-phase deposition characteristics of PVD, DVD, and CVD on fiber bundles from a cross-section view. Although CVD is a highly promising technique to create high-quality coatings on fibers, traditional CVD metal depositions require either high temperature (>200 ^{o}C) or result in inadequate step coverage in complex structures with higher than 10:1 aspect ratios.[63] Therefore, further development of CVD metal deposition technique is needed to bring CVD to practical use for polymer fiber metallization applications. In chapter 5 of this thesis, we report the utilization of DLE-CVD technique for the metallization of polymer fibers and fiber bundles, as well as the characterizations of coated fibers and their potential applications in flexible electronics.

Chapter 2   Self-Smoothing Al-Catalyzed SiO₂ ALD Process for Smooth-Wall Vertical Trench Structures with Ultrahigh Aspect Ratios

2.1   Introduction

In modern ultra-large-scale integrated (ULSI) architectures, blocks with different functionalities are connected three-dimensionally. Thus, semiconductor devices and interconnects must be made inside structures with high aspect ratios.[64-65] For example, fin-type field-effect transistors (Fin-FET) with high-aspect-ratio silicon fins need conformal coating of dielectrics, amorphous silicon (a-Si) gate, as well as the metal contacting with a-Si gates, as illustrated in Figure 2.1(a). Also, in multi-layer electronics, long through-silicon vias (TSVs) with ultra-small diameters are necessary to form contact with silicon devices on the substrate, as in Figure 2.1(b).[66] All these architectures require proper designing and fabrication of complex high-aspect-ratio structures.
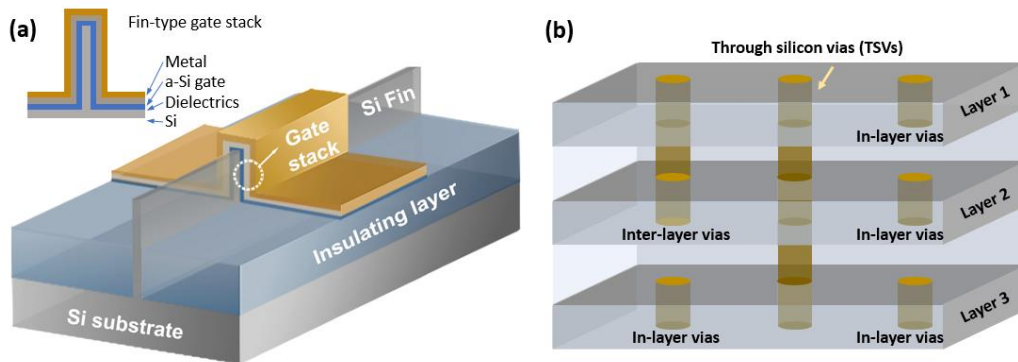

Figure 2.1. (a) Schematic illustration of conformal gate stack coating applied on Fin-FETs; (b) Vertical vias, including through silicon vias (TSVs), formed inside high-aspect-ratio hole structures in multi-layer silicon devices.

In traditional semiconductor industry, 3D high-aspect-ratio interconnects are very difficult to process because of the anisotropic nature of industrially available physical vapor deposition techniques.[67] Moreover, to achieve 3D microelectronic architectures, complex structures need to be fabricated on silicon substrates. In manufacturing, these structures can serve as the template for the formation of high-aspect-ratio metal interconnects. While in research and development, these structures can be used as test structures to evaluate step coverage of a conformal deposition technique like DLE-CVD.

There are many strategies to fabricate high-aspect-ratio structures on silicon substrates.[68] For example, uniform vertical trenches with aspect ratio as high as 16:1 can be fabricated by a metal-assisted chemical etching (MaCE) method.[69] This method involves a wet chemical etching process with $HF-H_2O_2$ and pre-patterned gold thin film catalyst. The gold catalyst increases the etching rate at Au-Si interface, thus resulting in vertical trenches after a certain amount of time. However, this method cannot remove the gold catalyst at the bottom of the trench, and involves wet chemistry that may not be compatible with other microelectronic fabrication processes. Another strategy is the Bosch-type deep reactive ion etching (DRIE). The DRIE process is conducted under vacuum, with pulsing gases alternating between C_4F_8 and SF_6.[70] C_4F_8 provides a conformal protective coating, then a vertically accelerated SF_5^+ ion beam is applied to bombard the bottom of the trench. After repeating the two steps for certain number of cycles, a deep trench structure with a desired high aspect ratio can be achieved.

Although this method requires complicated RIE apparatus, it provides better

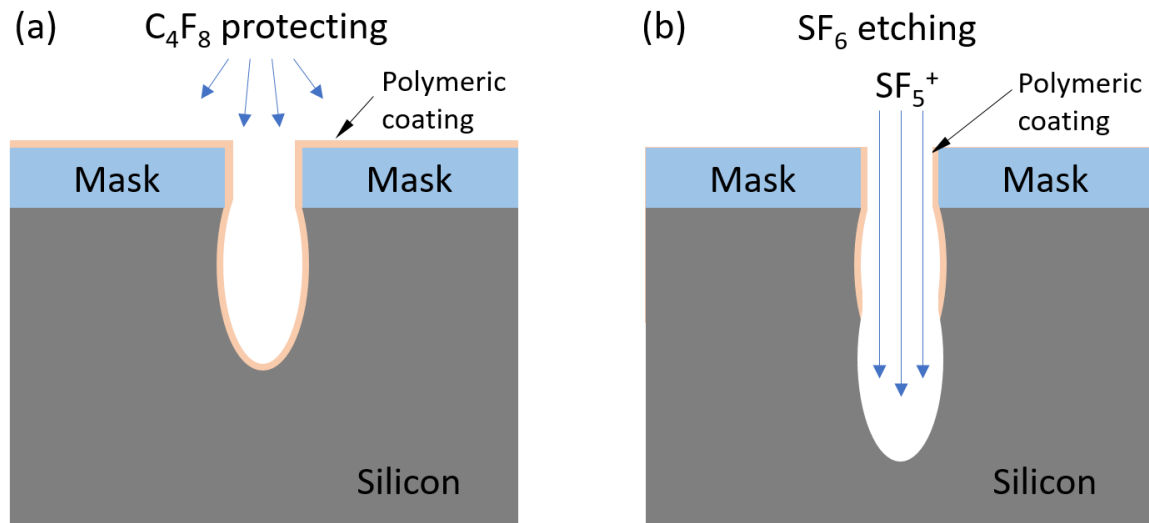controllability than wet chemical methods.

Figure 2.2. Schematic illustration of a Bosch-type RIE process. (a) Formation of

conformal C_4F_8 protective layer; (b) Vertical etching by SF_5^+ to form trenches.

As illustrated in Figure 2.2, the Bosch-type RIE mechanism creates trench structures

by forming small scallops stepwise, which introduces intrinsic roughness to the side

wall. These scallops are usually at the scale of tens of nanometers, which is smaller than

the size of previous interconnect vias. However, when ultrafine vias smaller than 20 nm

are needed in current and future electronics, these scallops will be a concern.

To crease smoother side walls, we used an Al-catalyzed SiO_2 atomic layer deposition

(ALD) process to smoothen these scallops. Interestingly, at the scale of 50-100 nm, the

Al-SiO_2 ALD process exhibits a self-smoothing effect, which is similar to the super-

conformal behavior as discussed in Chapter 1 Figure 1.4 and Figure 1.5. This super-conformal coating phenomenon is not common for ALD processes because ALD is a self-limited conformal process, which maintains the substrate morphology during the deposition process. Therefore, an investigation into this phenomenon has high scientific significance, and may create new methods to process complex high-aspect-ratio structures with the benefit of this self-smoothing effect.

In this chapter, various kinds of high-aspect-ratio structures are produced by lithography and RIE processes. parameters and methods for these processes are discussed in-detail. An Al-catalyzed SiO_2 ALD process is used to coat the etched structures to further increase their aspect ratios, as well as to smoothen the side walls. To evaluate the self-smoothing effect of Al-catalyzed SiO_2 ALD, special structures with controlled scallop patterns are fabricated as test structures. A possible mechanism for the self-smoothing effect is also proposed to explain the process.

2.2   Fabrication of High-Aspect-Ratio Structures by Reactive Ion Etching (RIE)

To fabricate high-aspect-ratio test structures, proper patterning of silicon substrates is needed to create masks for the RIE process. Usually, photoresist and e-beam resist can be directly used as a "soft mask", while in some cases where higher etching selectivity is required, SiO_2 or Si_3N_4 are used as "hard masks".[71]

Photolithography can produce micron-scale patterning in a short period of time, while e-beam lithography can produce nanometer-scale patterning but with longer

process times. For initial RIE process development, we used e-beam lithography to create well-defined trench patterns with PMMA resist (Figure 2.3 shows an example of photoresist soft mask for RIE process). It is noted that a proper e-beam exposure time (thus a better-defined pattern profile) is important to achieve smooth trench profiles. As shown in Figure 2.4, when the e-beam resist is over-dosed or under-dosed, irregular scallops or tapering effect were observed. Our best results were obtained with 700 uC/cm^2 dosage and 500 nm 950PMMA C4 e-beam resist.
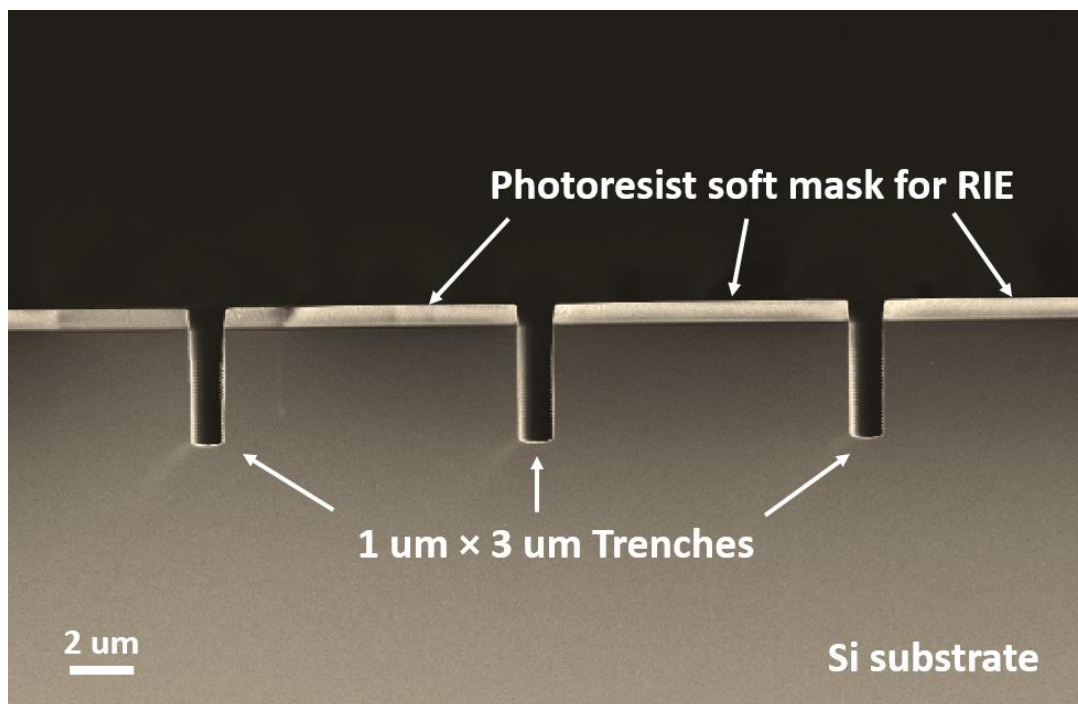
Figure 2.3. Using photoresist as soft mask for RIE etching process.
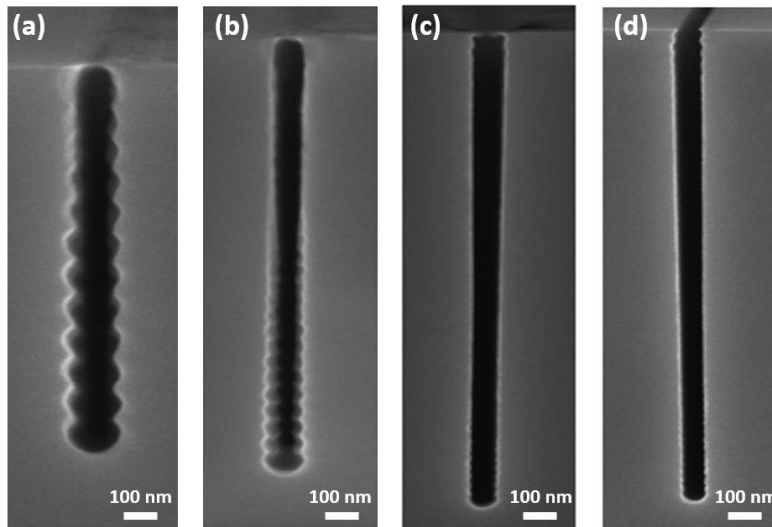
Figure 2.4. Trench structures that were patterned by different e-beam exposures with 200 nm 950PMMA C4 e-beam resist. (a) 500 uC/cm^2; (b) 600 uC/cm^2; (c) 700 uC/cm^2; (d) 800 uC/cm^2;
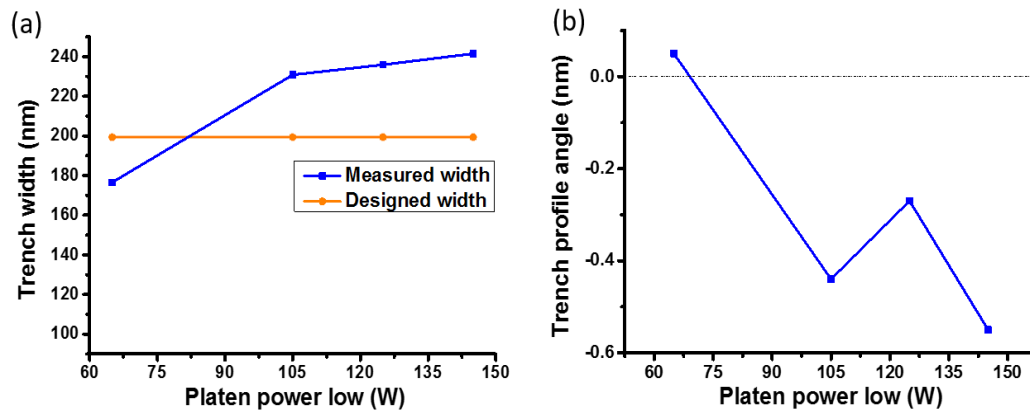
Figure 2.5. Platen power test. (a) Trench widths at middle depth with different platen powers; (b) Trench profile angles with different platen powers. All other parameters at kept the same for these tests: temperature (10 °C), etching cycle (1s C$_4$F$_8$, 1.2s SF$_6$, 30 loops), and 700 uC/cm^2 e-beam exposure dosage;

There are many RIE process parameters that have substantial impact on the etching results, including pulse numbers, platen power, and temperature, etc. We used slightly lowered temperature (10 °C) in RIE process for all our samples to avoid thermal diffusion of SF_6 which may reduce directional selectivity. Platen power is defined as the amount of power that SF_5^+ ions can obtain from the vertical bias applied to accelerate the ions. To study the effect of platen power on etched trench profile, we etched four samples with different platen powers, as shown in Figure 2.4. Generally, higher platen power leads to wider and more sloped trench (Plotted quantitatively in Figure 2.5). The best results were obtained with roughly 75 W lower limit and 140 W higher limit for platen power. Finally, with the optimized conditions, a 25:1 trench with slightly tapered side wall is demonstrated in Figure 2.6(a), while a 10:1 trench with perfectly vertical side wall is shown in Figure 2.6(b).
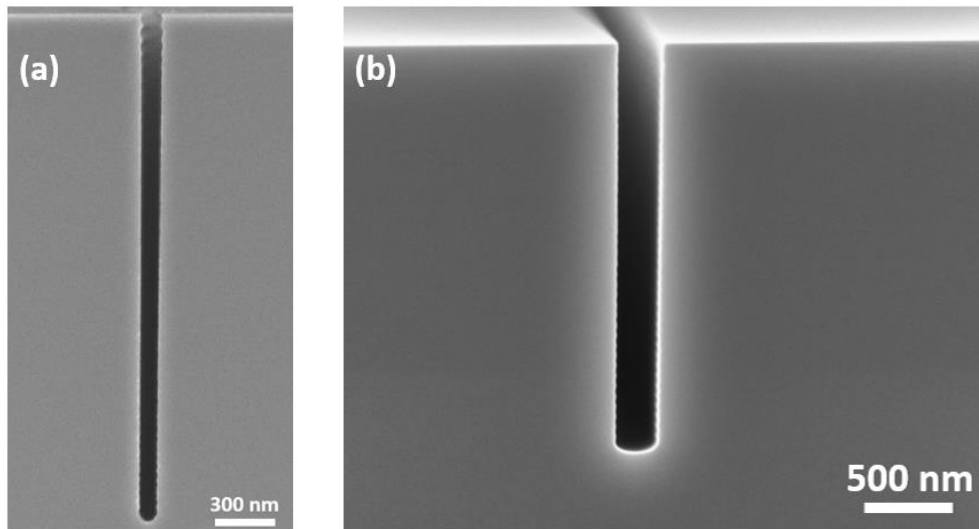
Figure 2.6. Trenches fabricated with optimized RIE processes. (a) 30:1; (b) 10:1.

To scale up the trench fabrication with photolithography, we used a design with arrays of holes, in which holes with different diameters and pitch sized are included, as shown in Figure 2.7. An interesting phenomenon observed on this sample is that the shapes of holes vary in blocks with different hole densities, even though the shapes of photoresist mask are perfectly circular. In our observation, the hole shape can remain circular at up to 8 holes/100 um^2, but become more square-like when the density reaches 32 holes/100 um^2. This is possibly due to a proximity effect during the RIE process, similar to the proximity effect known in e-beam lithography processes.[72]
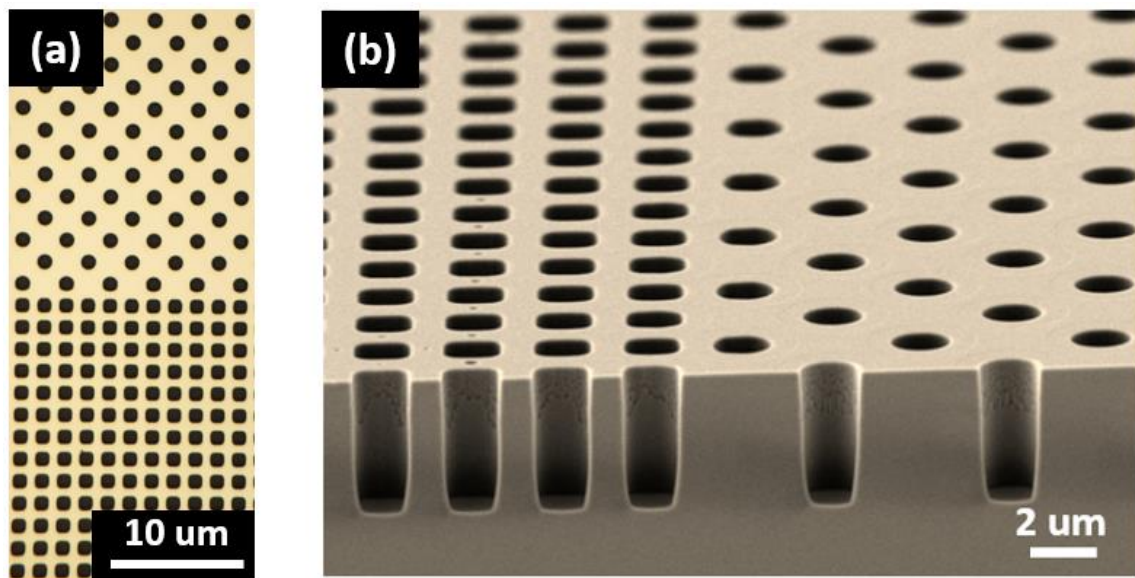
Figure 2.7. (a) Top-down optical image of the hole structures; (b) Cross-section SEM of the hole structures fabricated by photolithography and RIE process.

2.3 Al-Catalyzed SiO₂ ALD on High-Aspect-Ratio Structures

2.3.1 Al-Catalyzed SiO₂ ALD Process and Self-Smoothing Mechanism

The Al-catalyzed SiO₂ ALD process was developed in our group in 2002, and has been put into wide use in various kinds of commercial ALD systems as a standard high-efficiency SiO₂ deposition process.[73-74] As illustrated in Figure 2.8, this process involves two steps: The first step is exposing the sample surface to trimethylaluminum (TMA) vapor to form a monolayer terminated with -AlCH₃ groups, which is the same chemical process as in regular Al₂O₃ ALD; The second step is introducing large or multiple doses of *tris*(*tert*-butoxy) silanol precursor onto the -AlCH₃ terminated surface to form silicon dioxide layers on top of it.
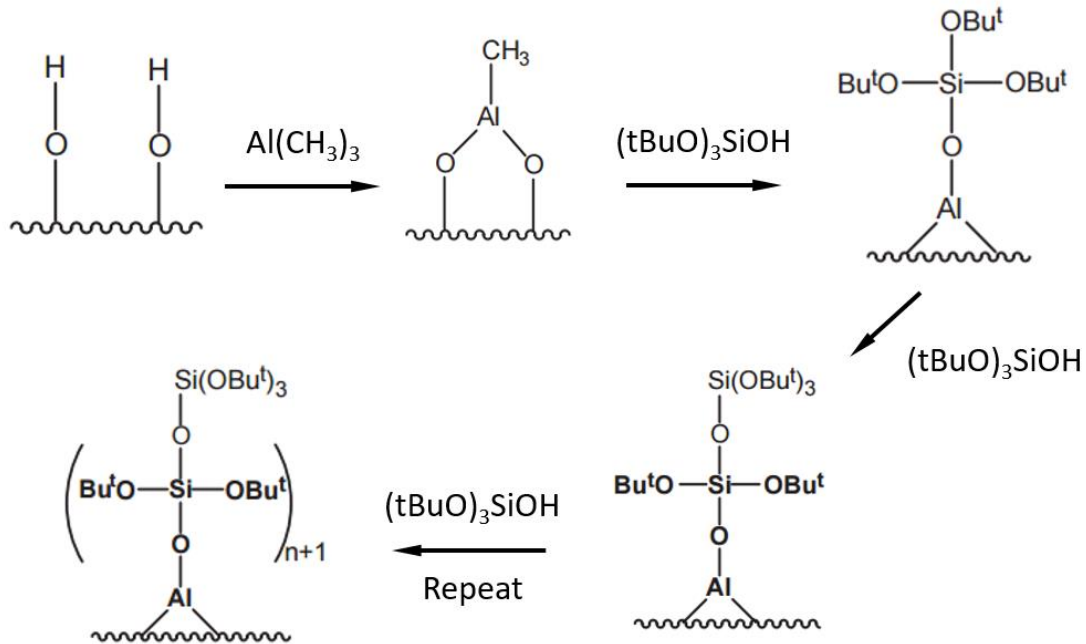
Figure 2.8. Al-catalyzed SiO₂ ALD process diagram.[73]
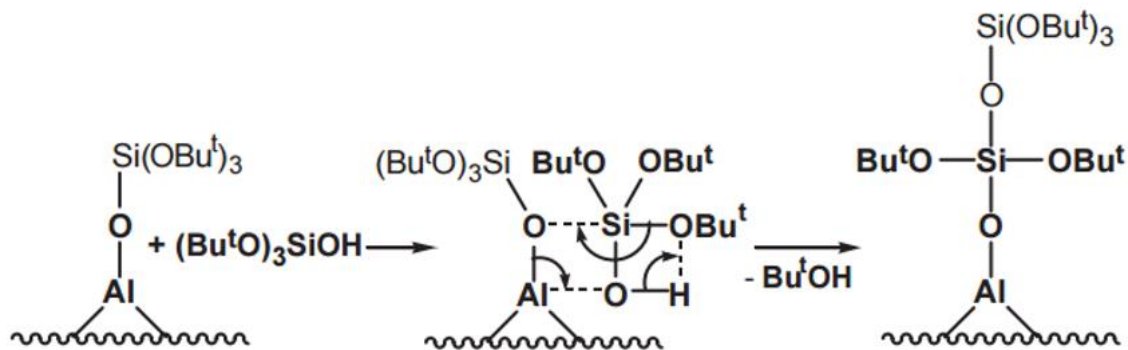
Figure 2.9. Al-catalyzing mechanism for Al-SiO$_2$ ALD process.[73]

Although the first step is a regular self-limited ALD process, the second step is not self-limited. After forming the first layer of -Al-O-Si(OtBu)$_3$, the silanol precursor dosed onto the sample surface will keep reacting at the bottom Al-O-Si area and form long chains of Al-O-(Si-O)$_n$, as shown in Figure 2.9. With the Al-catalyzing mechanism, the Al-SiO$_2$ process can happen much faster (>1 nm/cycle) than conventional ALD (~0.1 nm/cycle).

By doing Al-SiO$_2$ deposition on a zig-zag rough surface, we found that this ALD process can smooth out the rough surface as demonstrated in Figure 2.10. After deposition of ~130 nm Al-SiO$_2$, the roughness (defined as the average height difference between the bottom to apex of the zig-zag texture) of patterned Si test substrate decreased from ~47 nm to ~15 nm (68 % decrease). We call this phenomenon the self-smoothing effect of Al-catalyzed SiO$_2$ ALD. This effect can be observed when doing deposition onto surfaces with 20 ~ 200 nm features.
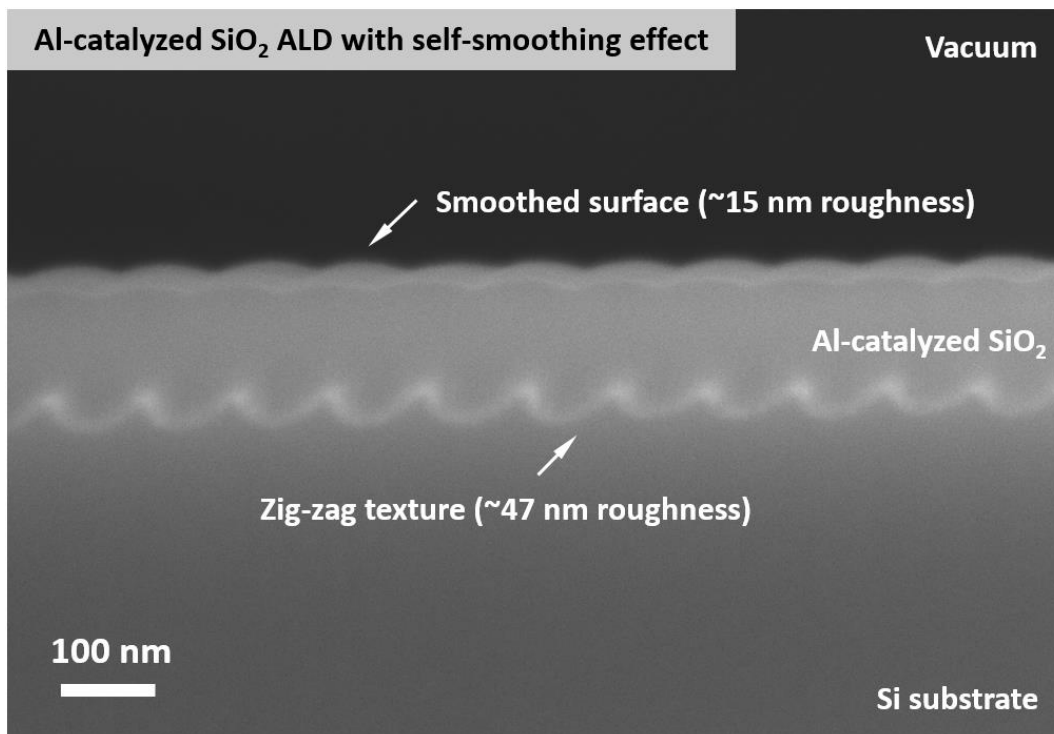
Figure 2.10. 130 nm of Al-catalyzed SiO_2 ALD thin film deposited onto a Si substrate with zig-zag textures on the surface, reducing the surface roughness (average peak to valley depth) 68 % from ~47 nm to ~15 nm, showing self-smoothing effect.

As a control experiment, we performed conventional Al_2O_3 ALD with trimethylaluminum (TMA) precursor on the same sample surface. During the deposition process, substrate temperature was set to 250 °C, base pressure was 200 mTorr, and carrier gas flow is 20 sccm of N_2. A cross-sectional SEM image of the resulting sample is shown in Figure 2.11. After coating the surface with ~130 nm by conventional Al_2O_3 ALD, the zig-zag morphology was mostly maintained (< 5 % roughness change from 43 nm to

41 nm), indicating that this process is a strictly self-limited conformal ALD process that replicates the initial morphology of samples.
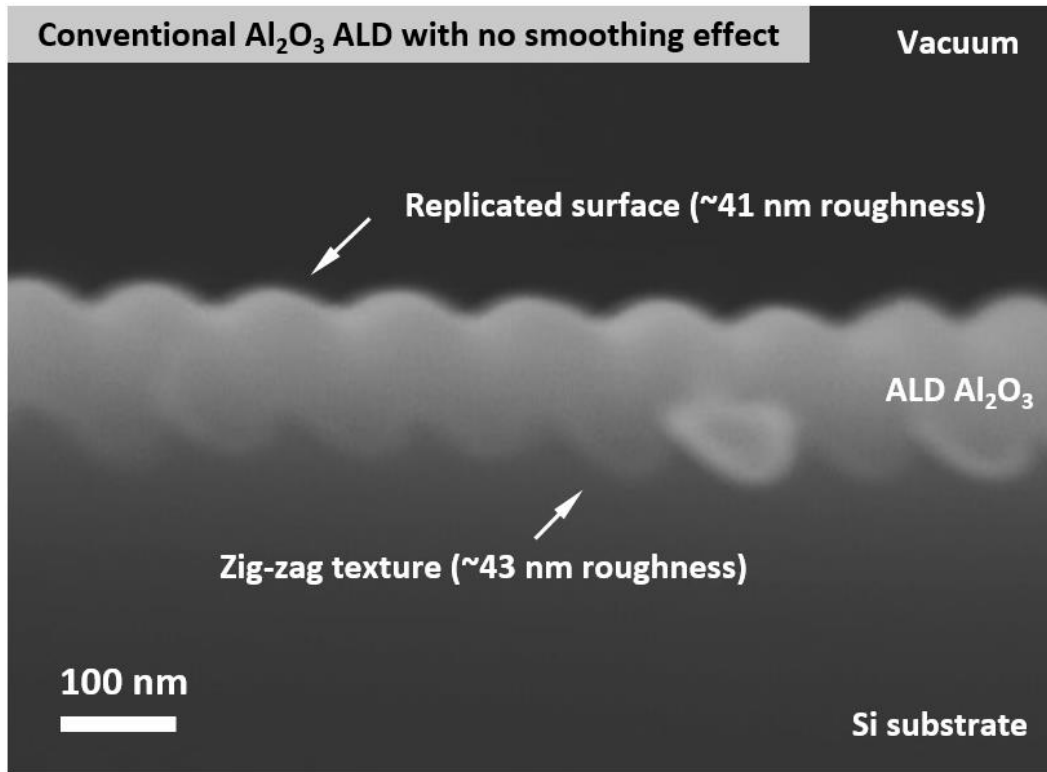
Figure 2.11. 130 nm of conventional Al_2O_3 ALD (with TMA precursor) deposited onto a Si substrate with zig-zag textures on the surface, creating a mostly replicated surface with less than 5 % change in surface roughness from ~43 nm to ~41 nm.

To better understand the Al-SiO_2 deposition process, we propose two possible mechanisms for the self-smoothing effect. The first proposed mechanism is "concave filling", as illustrated in Figure 2.12. Al-catalyzed SiO_2 ALD process produces polymer-like

chains of SiO_2 in each cycle. When performing this deposition on a concave substrate, those SiO_2 chains in the valley tend to touch each other and crosslink some of the chains. Therefore, the film near the bottom of a valley will be slightly thicker than the film deposited on planar surfaces. After repeating the process for multiple layers, the valley will be gradually filled up from the bottom and smooth out the surface. This mechanism is based upon a nanometer-scale perspective (each SiO_2 chain formed in an Al-SiO_2 ALD cycle is usually 1~5 nm), which can explain that the phenomenon is mostly easily observed on substrates patterned with 20 ~ 200 nm features.
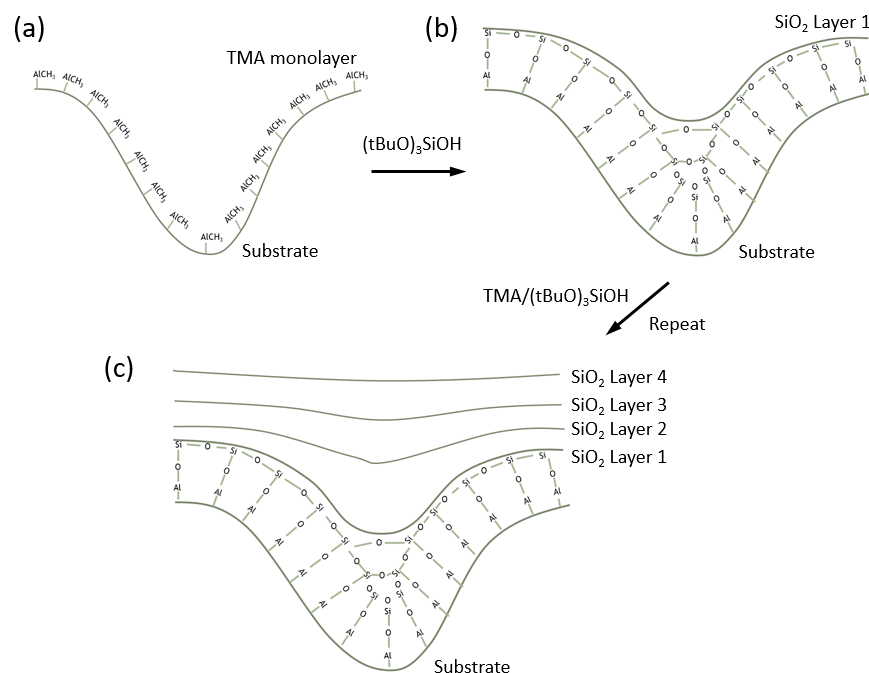
Figure 2.12. The proposed "concave filling" mechanism scheme. (a) A concave surface with a monolayer of TMA precursor attached; (b) Formation of long vertical SiO_2 chains on each Al site, causing the chains near bottom to touch and terminate each other; (c) After repeating the process, the surface gradually becomes smoother.
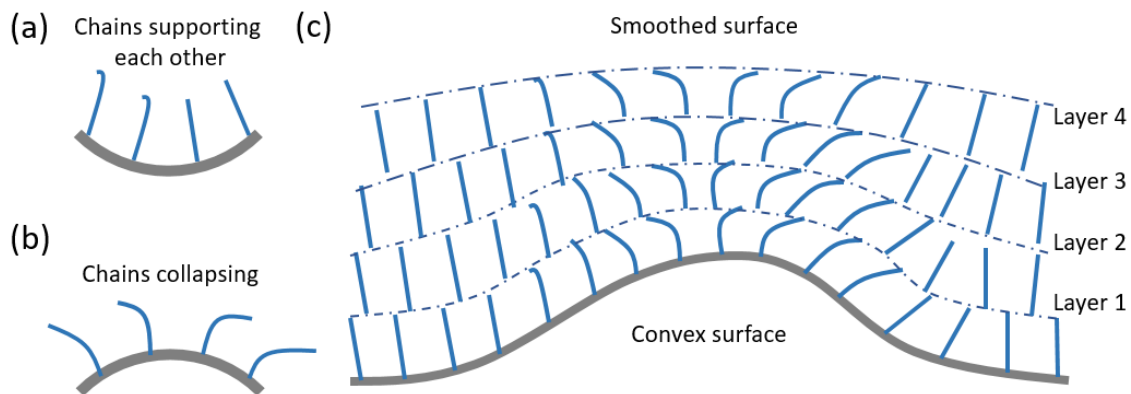
Figure 2.13. The proposed "convex collapsing" mechanism for the self-smoothing effect of Al-catalyzed SiO_2 ALD process. (a) SiO_2 chains support each other when deposited onto a concave surface; (b) SiO_2 chains are easier to bend and collapse when formed on a convex surface due to the lack of support from surrounding chains; (c) Illustration of the overall smoothing effect after repeating the process for multiple layers.

Another possible explanation is the "convex collapsing" mechanism. In the Al-catalyzed ALD process, long SiO_2 chains will have a certain degree of flexibility because each chain starts growth from a single Al center and extends upward, which is similar to the growth process of nanowires.[75] When formed on a concaved surface, the chains tend to mechanically support each other, and maintain a vertical growth behavior, as shown in Figure 2.13(a). However, when it comes to the scenario on a convex surface as in Figure 2.13(b), SiO_2 chains are growing without as much mechanical support from the surrounding chains. Thus, the chains formed on convex surfaces tend to bend and

31

collapse, resulting in a slightly thinner film near the apex of a convex surface than the film deposited on planar surfaces.

Figure 2.13(c) schematically illustrates the smoothing process by this mechanism, in which the top layers of the deposited film are getting flatter and flatter than the original convex substrate surface. This mechanism is based on molecular-scale processes, and can explain how the Al-catalyzed SiO_2 ALD is different from normal ALD processes. For example, in Al_2O_3 ALD process, TMA precursors are small enough to form a compact monolayer, and all active sites formed on both concave and convex sample surfaces have the same density, maintaining the same growth rate, thus the highly conformal deposition characteristics.

The overall self-smoothing phenomenon of Al-catalyzed SiO_2 may be caused by the combination of both "concave filling" and "convex collapsing" mechanisms. In short, the growth on lower parts of a rough sample surface is filled up faster than planar parts due to the geometry-induced crosslinking at the bottom, while the growth on higher part of a rough surface is slower because of the bending proneness of less-supported SiO_2 chains near peak areas. These mechanisms provide a qualitative explanation to the self-smoothing effect; however, more quantitative and thorough investigations are needed to better understand the process in the future.

2.3.2   Smooth-Wall Ultrahigh-Aspect-Ratio Trench Structures

As mentioned in the discussion of RIE mechanism in Figure 2.2, the Bosch RIE process intrinsically produces small scallops along the side wall of etched structures. Utilizing the self-smoothing effect of the Al-catalyzed SiO_2 ALD process, we can fabricate high-aspect-ratio structures with highly smooth side-walls. Of note, deposition of a conformal thin film in a trench can produce an even higher overall aspect ratio, because the process reduces the coated trench width while keeping trench depth the same. As a result, the aspect ratio can be readily controlled by changing the thickness of a deposited $Al-SiO_2$ film, which may be a benefit for industrial applications.
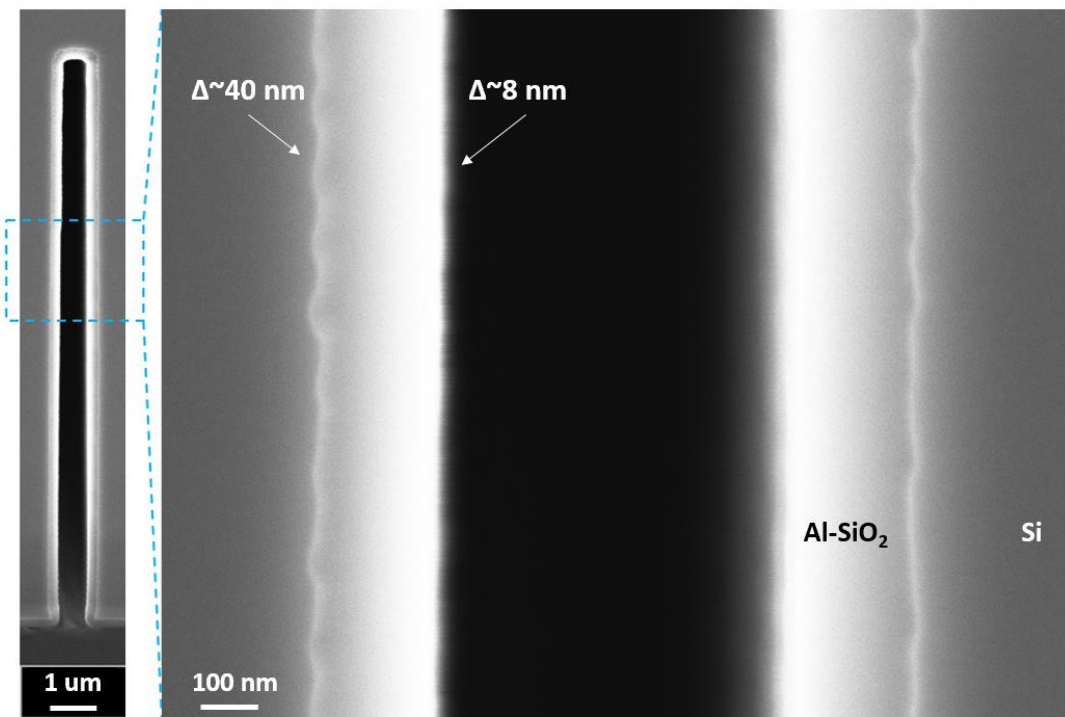
Figure 2.14. Al-catalyzed SiO_2 ALD reducing the side wall roughness of a rough-wall Si trench with 12:1 aspect ratio from ~40 nm to ~8 nm.

To demonstrate the application of Al-SiO$_2$ ALD for making smooth-wall, high-aspect-ratio structures, we fabricated Si trenches with rough side walls as test structures, and coated them with Al-SiO$_2$ ALD. In all these experiments, we used 250 °C substrate temperature, 200 mTorr base pressure, 4:1 silanol to TMA dosing ratio and 20 sccm N$_2$ carrier gas. Figure 2.14 shows the fabricated Si trench with ~40 nm surface roughness (average peak to valley depth). After coating the trench with 200 nm Al-SiO$_2$ ALD, the variation reduced substantially to ~8 nm.

(a) Original 20:1 Trench by RIE   (b) 30:1 Trench with 200 nm Al-SiO$_2$ (c) 100:1 Trench with 400 nm Al-SiO$_2$
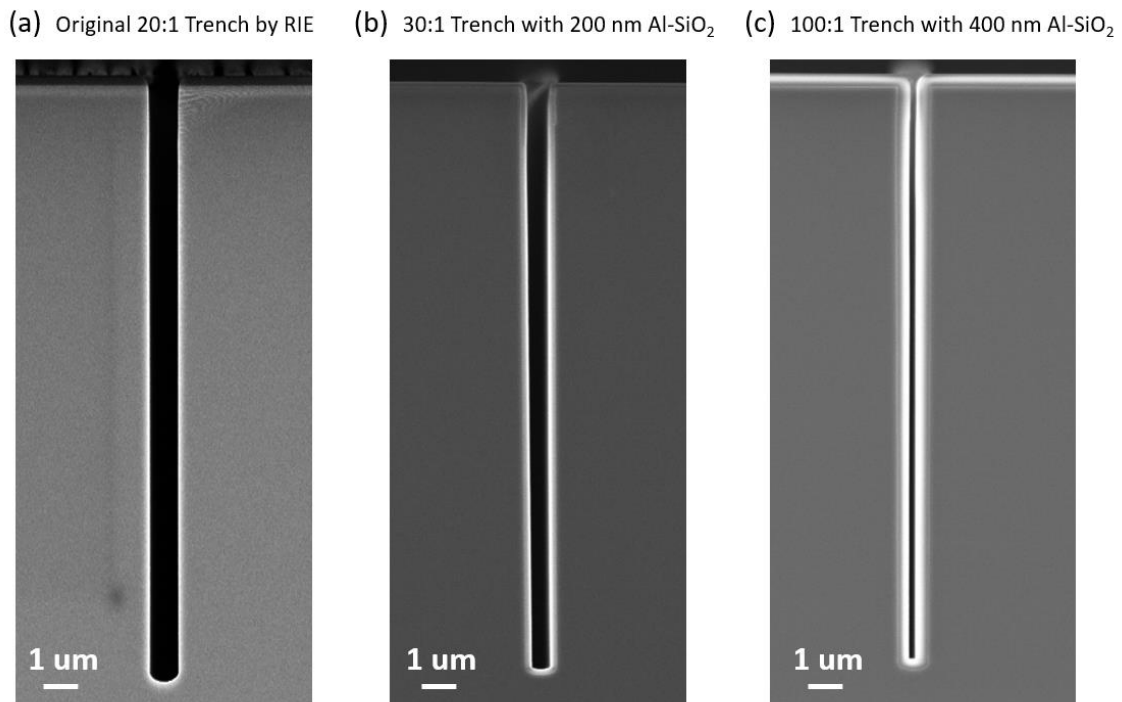
Figure 2.15. (a) Rough-walled Si trench with 18:1 aspect ratio fabricated by RIE process; (b) 30:1 aspect-ratio Si trench with smoothed wall by depositing 200 nm Al-SiO$_2$; (c) 100:1 aspect-ratio Si trench with smoothed wall by depositing 200 nm Al-SiO$_2$.

Here we also demonstrate that highly controllable smooth-walled trenches with increased ultrahigh aspect ratios can be fabricated. Figure 2.15(a) shows an 18:1 aspect-ratio Si trench fabricated by RIE process, which has a ~40 nm side wall roughness. After depositing 200 nm Al-catalyzed SiO_2 ALD thin film onto the trench, the side wall roughness reduced to ~8 nm, and aspect ratio increased to 30:1, as in Figure 2.15(b). Further deposition of a total of 400 nm Al-SiO_2 gives a ~6 nm side wall roughness and an ultrahigh 100:1 aspect ratio, as presented in Figure 2.15(c). Al-SiO_2 thickness dependence of the trench side wall roughness is plotted in Figure 2.16. Of note, the trench width of the final 100:1 trench is highly uniform throughout the entire structure, indicating that this method is promising for the fabrication of smooth-wall, complex structures with even higher aspect ratios.
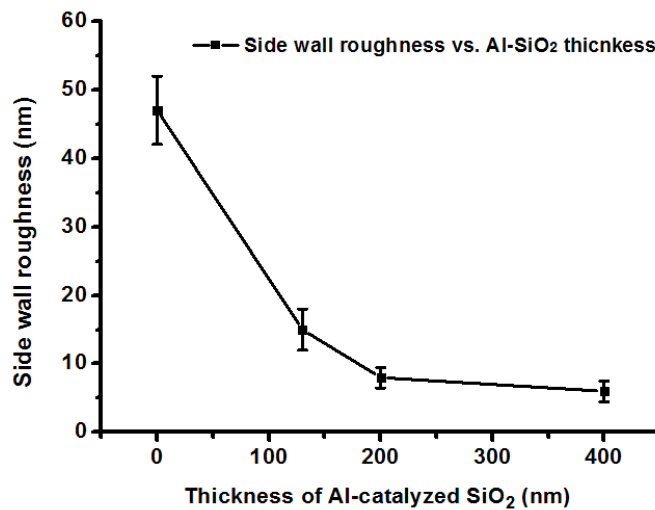
Figure 2.16. Trench side wall roughness versus the thickness of coated Al-SiO_2. The error bar indicates the deviation of peak-to-valley depth of each scallop on trench side wall.

2.4   Conclusions

In this chapter, we described fabrication processes to make smooth-wall, high-aspect-ratio structures based on reactive ion etching (RIE) and a self-smoothing Al-catalyzed SiO$_2$ deposition method. The Bosch RIE process is a highly effective and controllable way to create trench structures with desired width and depth, but it introduces intrinsic side wall roughness due to its cycling etching mechanism. As a solution to this issue, Al-catalyzed SiO$_2$ deposition can reduce the side wall roughness of these structures by at least 68 %, while conventional Al$_2$O$_3$ ALD of similar thickness brings less than 5 % roughness decrease on the same structure. Moreover, coating a specific thickness of Al-catalyzed SiO$_2$ can controllably increase the overall aspect ratio of the fabricated structures up to at least 100:1. These studies provide strategies to develop evaluation platforms to study conformal thin film deposition processes, and provide methods to create high-quality complex structures for three-dimensional architectures with ultrahigh aspect ratios. Such structures could enable the production of future semiconductor electronics or optical devices.

Chapter 3   DLE-CVD of Nano-Crystalline Cobalt Metal for Nanoscale Copper Interconnect Encapsulation

3.1   Introduction

Continued progress in the downsizing of microelectronic devices has brought great challenges in many fields, especially interfacial engineering and interconnect fabrication at nanometer scales.[76-77] As a critical part of transmitting signals among microelectronic units, metal interconnect architectures have been calling for exponentially increased integration density and complexity in the past decades.[78] One of the greatest obstacles limiting the industry from further scaling down copper (Cu) interconnects, which is the most widely used interconnect material, is the electromigration (EM) and diffusion of Cu.[3, 79-80] Various barrier, liner and capping layers for Cu interconnects have been reported in the effort to stabilize Cu atoms by suppressing their diffusion and migration, including SiNx, SiCN and transition metal nitrides.[81-83]

However, when it comes to a 22 nm technology node and below, dimensions of interconnects are already less than the mean free path (MFP) of Cu (~40 nm), while Cu metal conductivity decreases exponentially as it shrinks in size below MFP due to surface and grain boundry scattering.[84-86] As a result, by adding several nanometers of a low conductivity tantalum nitride barrier layer (~10^6 S/m) onto Cu (5.96×10^7 S/m), the effective width of a Cu wire would be decreased by 10 − 20 %, thus drastically decreasing the overall conductivity of the nanoscale interconnects.[87-88] Therefore, a

high-conductivity metallic material with Cu stabilization functionalities is needed for further-down-sized microelectronic interconnects.

Cobalt (Co) and Co alloys are known as effective capping layers that are capable of suppressing surface electromigration of Cu at macroscopic scales.[89-90] Furthermore, since Co has a high bulk metallic conductivity of 1.60×10^7 S/m and an estimated MFP of only ~16 nm at room temperature, it is emerging as a promising candidate for advanced Cu liner/capping layers.[91-92] Traditionally, Co metal was deposited by PVD methods that do not have the capability of coating inside high-aspect-ratio structures.[93] Thus, metal-organic chemical vapor deposition (MOCVD) with cobalt carbonyl precursors [e.g., $Co_2(CO)_8$] was introduced for better conformality.[94] However, cobalt carbonyl precursors have poor thermal stability and narrow practical deposition temperature windows, and usually lead to a rough film with surface roughness rms greater than 2.2 nm.[95] Recently, our group reported novel direct-liquid-evaporation chemical vapor deposition (DLE-CVD) methods for metal and metal nitride thin films, which provided the feasibility to create higher-quality Co films over a wide range of deposition temperatures and low chance of pre-deposition decomposition of precursors.[39, 42]

When a precursor is vaporized from a conventional bubbler, the actual rate of vapor delivery is subject to many variables, including drifts in the bubbler temperature, the amount of precursor remaining in the bubbler, and thermal decomposition during long times at high temperatures. In contrast, precursors in DLE-CVD systems are stored at room temperature, such that thermally-induced decomposition is negligible. The

residence time of the precursor vapor in the heated evaporation region is also very short, minimizing the decomposition of the precursor during the vaporization. The precursor delivery rate is stably controlled and measured by a liquid flow-controller immediately before it flows into the evaporation region.[96] In making nanoscale metal interconnects, it is critical to have precise control over all deposition processes in order to guarantee reliability and reproducibility. For liners and capping layers of copper interconnects, it is particularly important to design deposition conditions that create continuous and pinhole-free films with nano-sized crystallinity for blocking the diffusion of copper.[97]

In this chapter, we use nanoscale elemental imaging and electrical measurements to demonstrate that precisely controlled DLE-CVD of Co metal films is a promising liner and capping layer for nanoscale Cu interconnects. Narrow Cu wires encapsulated all-around by DLE-CVD Co were fabricated as illustrated in Figure 3.1. In-depth study of temperature-dependent deposition characteristics and atom probe tomography (APT) analysis are conducted to understand better the kinetics of DLE-CVD Co growth and its atomic-scale morphology. Morphological studies showed that our DLE-CVD Co forms a smooth nanocrystalline film with a grain size of ~10 nm and surface roughness rms of ~0.9 nm. Electrical measurements on microcapacitors show that Cu is effectively blocked from diffusing into the SiO_2 dielectric layer by our DLE-CVD Co.

This work provides direct evidence that encapsulating nanoscale Cu interconnects with nanocrystalline DLE-CVD Co can substantially improve its stability and suppress

diffusion of Cu atoms, paving the way for improved Cu interconnects in advanced microelectronics.
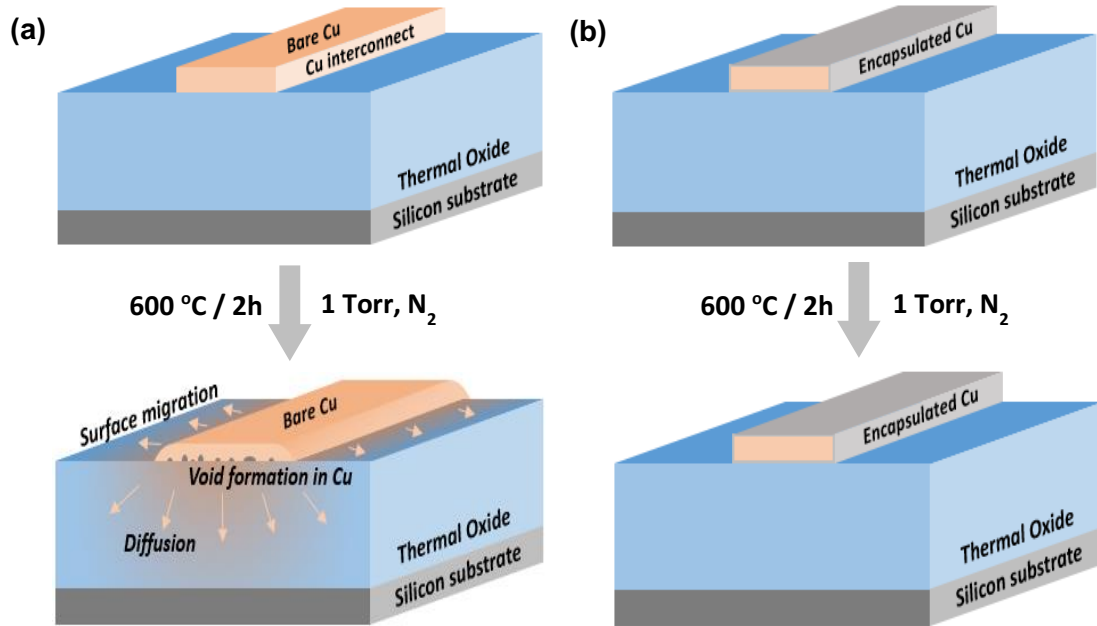
Figure 3.1. Schematic illustration of preventing the diffusion and deterioration of nanoscale Cu interconnects by DLE-CVD Co encapsulation. (a) Bare Cu interconnect; (b) Cu interconnect with DLE-CVD Co encapsulation.

3.2   Experimental Methods

The precursor used in this work is a cobalt amidinate, bis(N,N'-diisopropylacetamidinato) cobalt(II) (Figure 3.2), which has been reported previously.[39,43] Tetradecane (Millipore Sigma Chemical Co.) was distilled from sodium to remove

moisture before use. All chemical operations were conducted in a glove box with a

nitrogen atmosphere. Cobalt precursor solution was prepared by dissolving 5 g of Co

precursor in 50 ml of tetradecane.
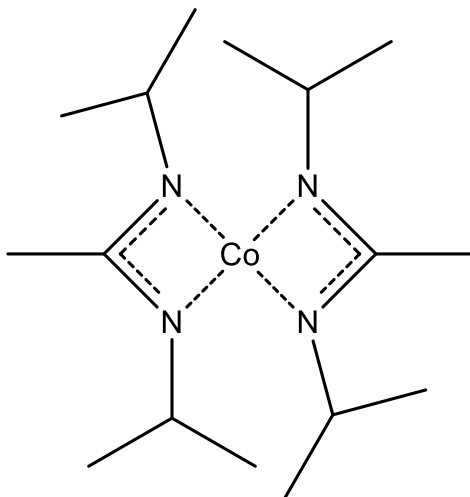
Figure 3.2. Co precursor for DLE-CVD Co depositions. Name: bis(N,N'-

diisopropylacetamidinato) cobalt(II).

The CVD of Co is conducted with a home-made direct-liquid-evaporation (DLE)

system (Figure 3.2). During the deposition process, a precisely controlled precursor

solution flow (12 wt% in tetradecane) is injected into and vaporized in a heated

vaporization loop, in which a constant 100 cubic centimeters per minute (sccm) of N_2 is

flowing as a carrier gas. Then the precursor vapor is mixed with 100 sccm purified

ammonia (NH_3) and 100 sccm hydrogen (H2) as co-reactant gases, and delivered into a

preheated deposition chamber (16-inch long and 1.25-inch diameter) with an 11 inch ×

1.25 inch semi-cylindrical sample holder inside. The total pressure in the reactor

chamber is also regulated and maintained at 10 Torr, in which the partial pressures of NH_3, H_2 and N_2 all equal 3.23 Torr. The Co precursor partial pressure varied from 0.02 Torr to 0.08 Torr in this work. Based on the calculation of reaction zone volume and flow rates, it takes roughly 13 s for a precursor molecule to be delivered across the reaction zone on statistical average.
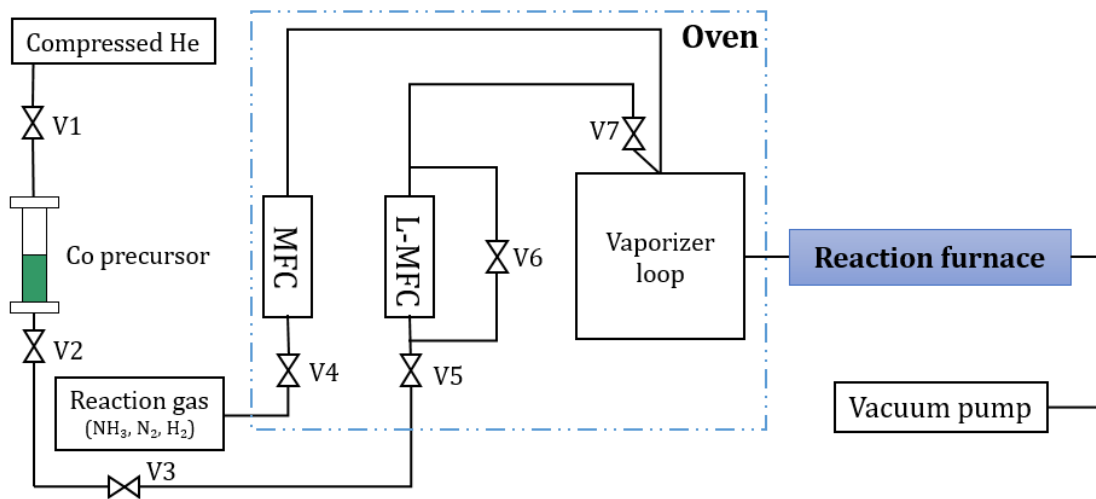
Figure 3.3. DLE-CVD Co System Diagram.

In order to evaluate the copper barrier performance of DLE-CVD Co, a p-type silicon chip with 50 nm thermal oxide layers was coated with 10 nm DLE-CVD Co at 200 °C followed by 50 nm PVD Cu, then annealed at 600 °C for 1 hour under 1 Torr of flowing N_2. After annealing, the Cu and Co films were removed by wet etching to fabricate micro-capacitors. 50 um x 50 um square-shaped Au electrodes were then fabricated by standard photolithography, metallization and lift-off process. For comparison, non-

annealed samples were also fabricated into micro-capacitors. The micro-capacitors were measured by a probe station with a Keysight E4980A precision LCR meter. Capacitance versus voltage (C-V) characteristics were measured at 2 MHz with a sweep rate of 0.2 V/s. All measurements started at positive 5 V and scanned from positive bias toward negative bias.

The cross-sectional morphology of the films was visualized with a Zeiss Ultra Plus field-emission scanning electron microscope (FE-SEM), from which the thickness of each film was measured. A Zeiss Ultra55 with EDAX detector was used to acquire EDAX mapping images. The depth-profile elemental analysis was carried out by Thermo Scientific K-Alfa X-ray photoelectron spectroscopy (XPS). A JEOL 2100 transmission electron microscope was used to study microscopic crystallography for which the samples were prepared onto a TEM grid with an ultrathin silicon nitride membrane. X-ray diffraction patterns were acquired by a Bruker D2 Phaser. Surface morphology of the films was analyzed by atomic force microscopy (AFM) (Asylum Model MFP-3D AFM system). Step coverage evaluation of DLE-CVD Co was conducted on a planar trench structure. The fabrication process for the planar trench test structure will be discussed in the next section. Nanoscale Cu lines for the demonstration of Co encapsulation were patterned by an Elionix F-125 ultra-high precision electron beam lithography system, and metallized by electron beam evaporation of Cu.

3.3   Characterizations of Nano-Crystalline Cobalt Thin Films

3.3.1   Growth Characteristics

For better understanding of the deposition process of DLE-CVD cobalt metal, we conducted a series of temperature-dependent studies. In all depositions, co-reactant gas flows are set to be 100 sccm NH_3 and 100 sccm H_2, and the precursor solution concentration is fixed at 12 wt%, which were evaluated to be the best conditions for high conformality and smoothness according to our previous report.[39]

Figure 3.4(a) plots the growth rates of DLE-CVD Co versus precursor solution flow rates at different temperatures. The results show that our deposition process is highly controllable by precisely setting precursor flow rates and temperatures. A lower temperature with a lower flow rate is suitable for nano-scale applications such as local interconnect and nanoscale capping layer, while a higher temperature with higher flow rate is favorable for larger-scale coatings such as intermediate and global interconnects in 3D microelectronics.[81] By plotting the natural logarithm of growth rate versus the reciprocal of temperature as shown in Figure 3.4(b), we calculated the activation energies of Co deposition processes with different precursor flow rates based on the Arrhenius' equation. Activation energy of the Co DLE-CVD deposition process is estimated to be 63.1 ± 1.2 kJ/mol on silicon substrates, which is in accordance with previous reports on thermal oxide substrates.[98-99]
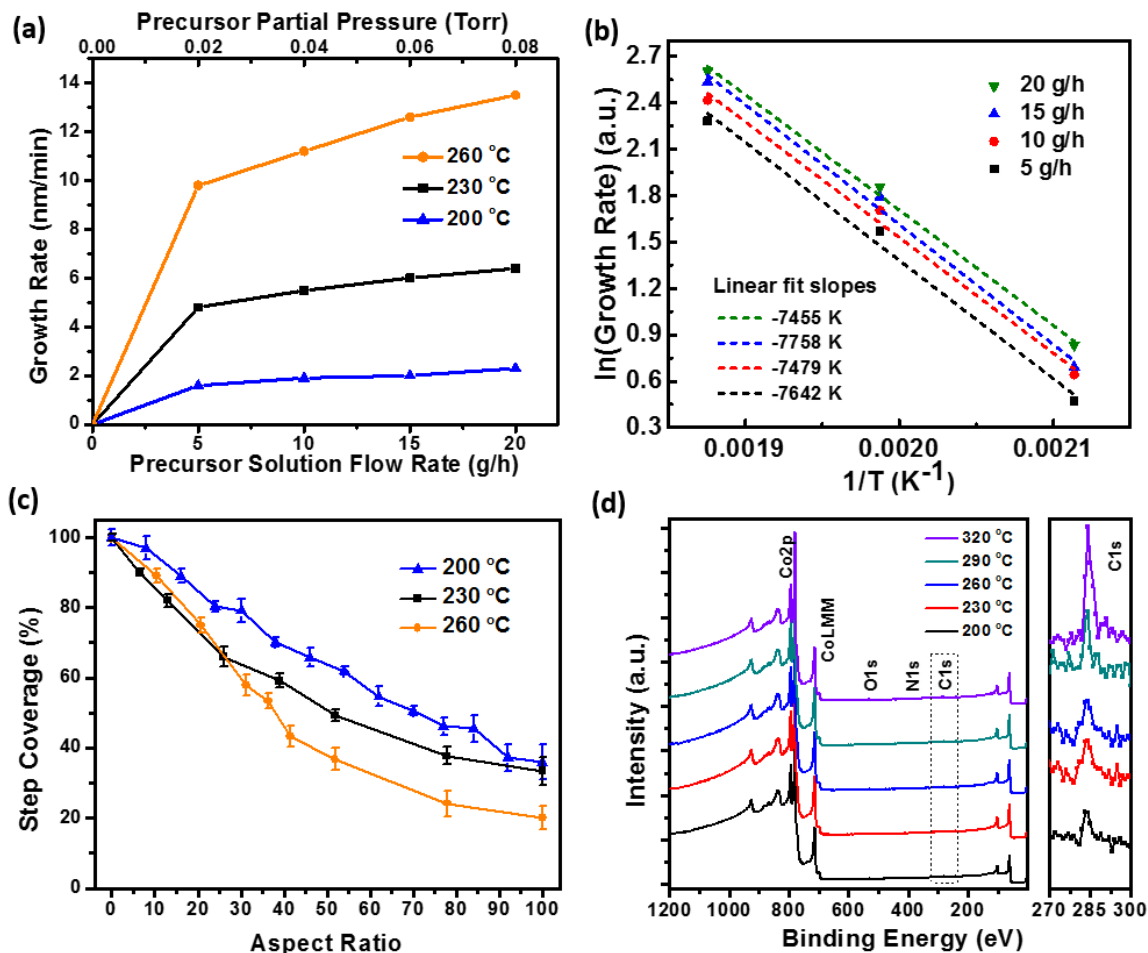
Figure 3.4. (a) Precursor flow-dependent growth rate plot at different deposition temperatures; Total pressure is 10 Torr in all experiments; (b) Arrhenius plots and linear fits at different precursor flow rates; (c) Step coverage along a horizontal trench test structure; (d) XPS survey scans of DLE-CVD Co samples deposited at different temperatures; the boxed region is the C1s peak, which is magnified on the right side.
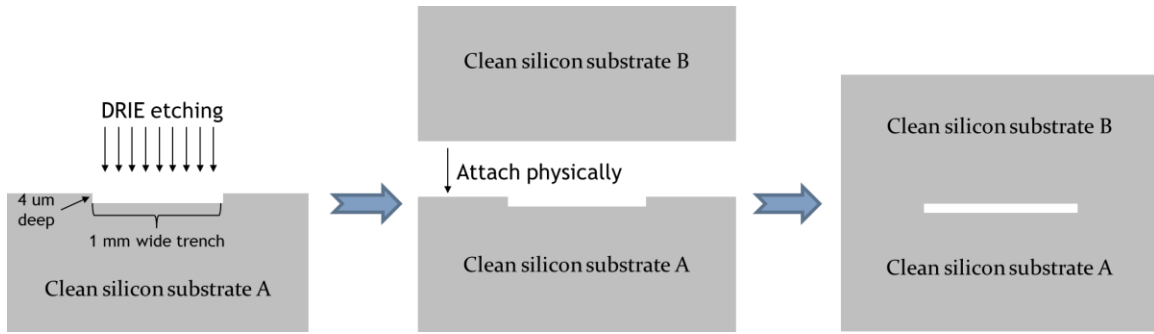
Figure 3.5. Schematic flow chart (cross-section view) of the fabrication process of

horizontal trench test structures on which step coverage evaluation for our DLE-CVD Co

deposition process is conducted.
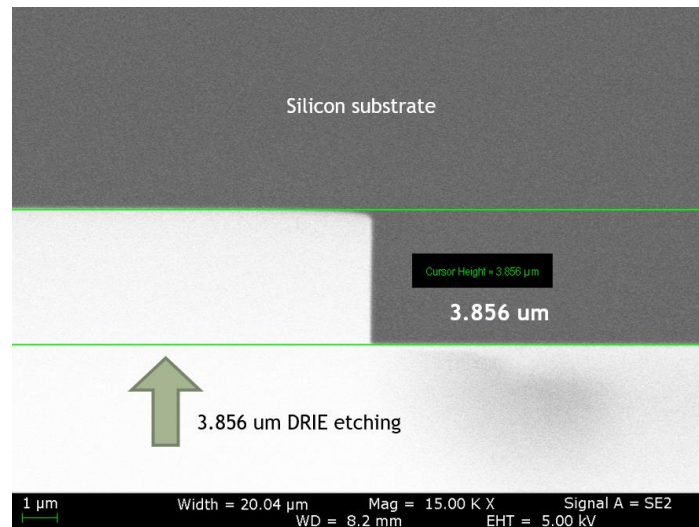
Figure 3.6. Cross-section SEM image of the planar trench test structure.

To demonstrate the step coverage of our DLE-CVD Co films, we developed a parallel

trench structure with an ultrahigh aspect ratio as a test platform, as illustrated in Figure

3.5. In the fabrication process, a flat silicon chip was first coated with 2 um of positive

photoresist as a soft mask, and patterned with 500 um wide 0.5 cm long exposed lines

by photolithography. A 500 um wide, ~3.86 um deep shallow trench (Figure 3.6) was created by a Bosch-type deep silicon reactive ion etching (DRIE) process with SF_6 and C_4F_6 gases, and thoroughly cleaned afterwards. Finally, the chip was physically capped with another flat silicon chip to cover part of the 0.5 cm length, leaving one end exposed as the opening of the parallel deep trench.
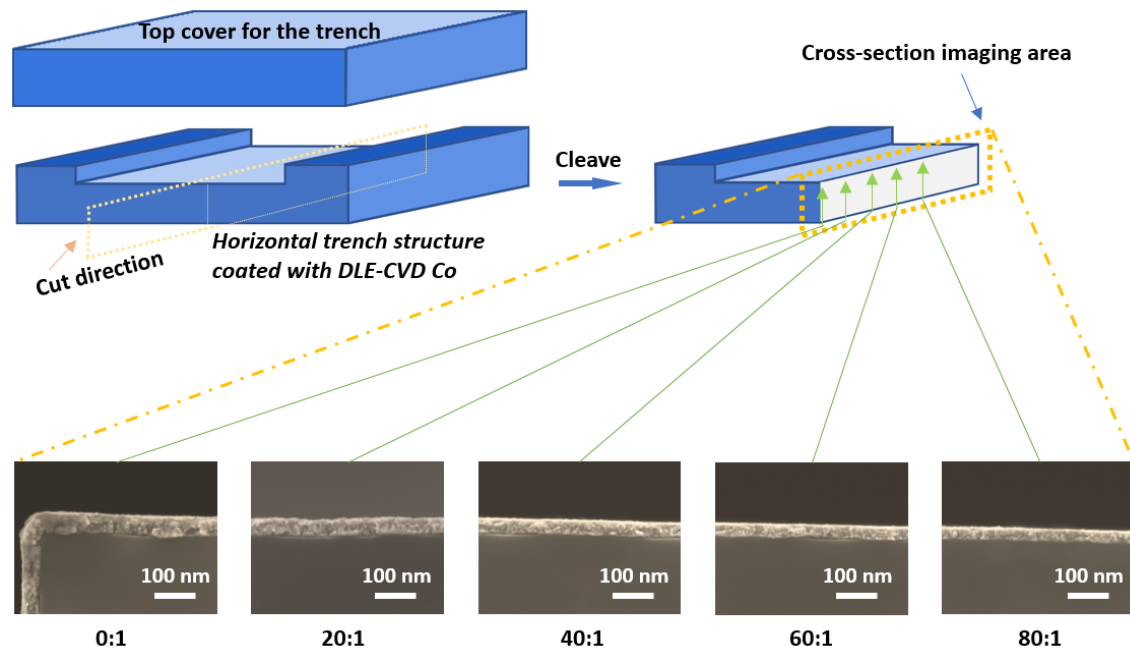
Figure 3.7. Schematic illustration of the assessment of step coverage on the horizontal trench test structure. The test structure was coated with DLE-CVD Co, then cleave along the direction of the horizontal trench. Then cross-section SEM imaging at different depth with different aspect ratios were conducted and measured thickness of Co layer. The DLE-CVD Co sample shown in the images was deposited at 200 ºC.

Co films were then deposited on the test structure by DLE-CVD at various

temperatures at a constant precursor flow rate of 5 g/h. Cross-section SEM images were

acquired to measure film thickness at different depths (as in Figure 3.7), showing that

our 200 °C film has over 95 % step coverage at a 10:1 aspect ratio, and maintains 50 %

step coverage even at a 70:1 aspect ratio. Moreover, based on the results shown in

Figure 3.4(c), 230 °C and 260 °C films both have over 90 % step coverage at a 10:1

aspect ratio, and maintain 50 % step coverage at 60:1 and 35:1 aspect ratios,

respectively.

### 3.3.2 Composition of DLE-CVD Co

In addition to high deposition rate and high conformality, low impurity level, e.g., low

carbon level, is also required for intermediate and global level interconnects because

carbon content can decrease the conductivity of metal interconnects, thus increasing

the energy consumption of overall device.[12, 67] X-ray photoelectron spectra (XPS) of DLE-

CVD Co samples deposited at different temperatures are provided in Figure 3.4(d). All

spectra are taken after 100 s of 100 eV Ar$^+$ sputtering to remove surface contamination.

Substantial amounts of C (>5 at%) are only observed in the samples deposited at above

290 °C. Samples deposited at temperatures up to 230 °C show less than about 1 at% of C

contamination. To estimate the impact of C content on DLE-CVD Co, we measured the

conductivity of Co films with different C contents, which is discussed in the supporting

information Table 3.1. The results show that the resistivity substantially increased when

the C content rose above 2 at%, indicating that the DLE-CVD Co films deposited at lower than 230 °C (< 1 at% carbon shown by XPS) will be more promising to achieve better performance as interconnect materials.

Table 3.1. Resistivity of DLE-CVD Co with different carbon contents

Deposition Temperature (°C)	200	230	260	290
Carbon Content (at%)	< 1	< 2	5	15
Resistivity (μOhm·cm)	25	30	100	195

3.3.3   Crystallinity and Morphology Studies of DLE-CVD Co

For Cu liner/capping layer applications, it is important to develop nanocrystalline Co films to ensure smooth surface coverage of Cu wires. APT results demonstrate the ultra-high purity and uniformity of our 200 °C DLE-CVD Co film, but do not provide information about microscopic surface morphology and crystallography. To study these characteristics, we performed transmission electron microscopy (TEM) and atomic force microscopy (AFM) imaging on the 200 °C sample. TEM image shown in Figure 3.8(a) reveals that the film is a nanocrystalline material with a grain size of around 10 nm. High-resolution imaging of lattice alignments at the grain boundary is included as the inset of Figure 3.8(a). More high-resolution TEM images are also provided in Figure 3.9. Tapping-mode AFM surface scan (Figure 3.8b) shows a rms surface roughness of ~0.9 nm, indicating that our DLE-CVD process produces highly smooth Co metal film.
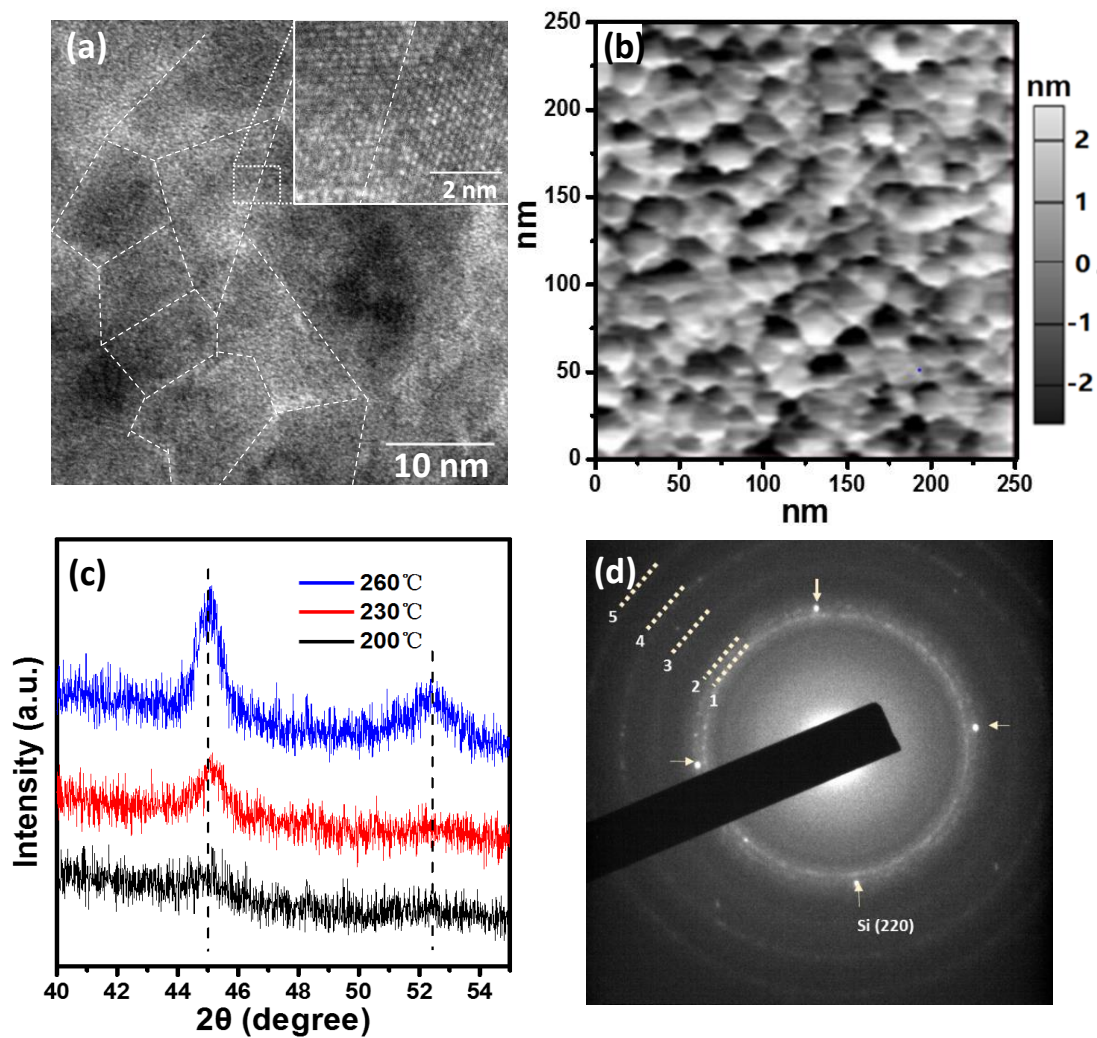
Figure 3.8. (a) TEM image showing the grain distribution of DLE-CVD Co deposited at 200 °C; (b) Tapping-mode AFM image of DLE-CVD Co deposited at 200 °C; (c) XRD pattern of DLE-CVD Co deposited at different temperatures, showing peak broadening at lower temperatures due to the formation of nanocrystallines; (d) ED pattern of DLE-CVD Co deposited at 200 °C, in which the 4 marked dots belong to Si (220) reference.
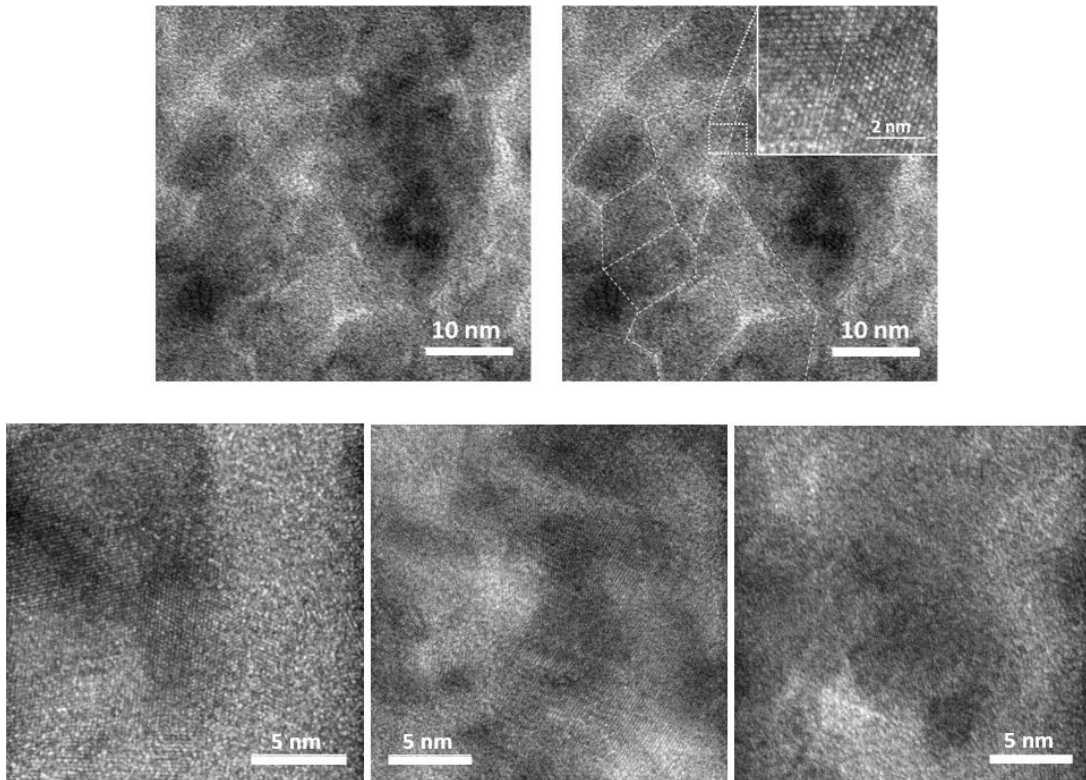
Figure 3.9. High-resolution TEM images of DLE-CVD Co deposited in 200 ^{o}C. Top two images show crystal domains without and with dashed lines as indicators of domain boundaries; Bottom three images are additional high-res TEM images in nearby areas.

X-ray diffraction (XRD) patterns of samples deposited at different temperatures (Figure 3.8c) reveal that with lower deposition temperatures, the DLE-CVD Co tend to form smaller-sized nanocrystals. Figure 3.8(d) presents the electron diffraction (ED) pattern of the 200 ^{o}C DLE-CVD Co sample, in which five major rings are observed. More ED patterns for DLE-CVD Co samples deposited at 200 ^{o}C, 230 ^{o}C and 260 ^{o}C are also presented in Figure 3.10.
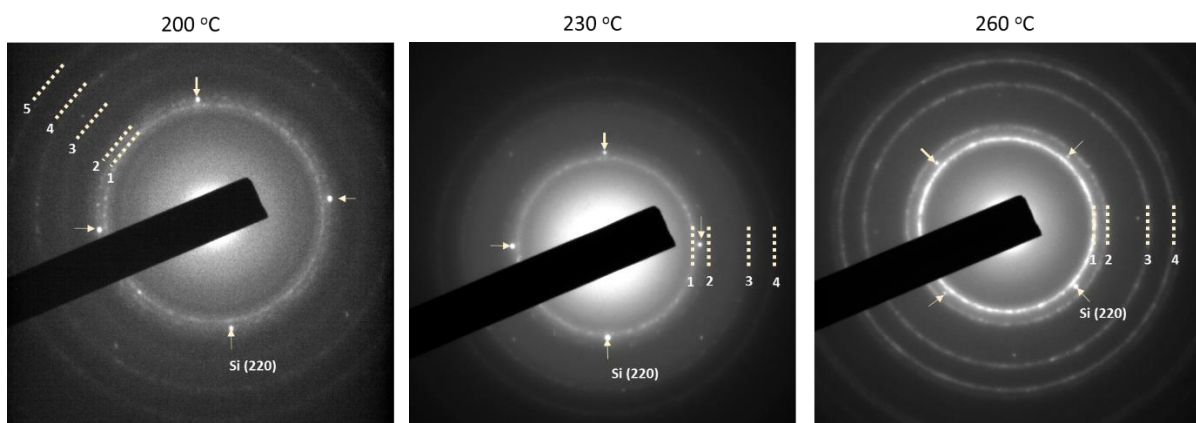
Figure 3.10. Electron Diffraction patterns for DLE-CVD Co samples deposited at different temperatures.

Based on these ED results, experimental and theoretical lattice parameters are summarized in Table 3.2 (200 °C), Table 3.3 (230 °C) and Table 3.4 (260 °C). Therefore, in Figure 3.8(d), ring 2 and ring 3 belong to hcp-Co (JCPDS 71-4239), ring 4 and ring 5 belong to fcc-Co (JCPDS 15-0806), and both phases contribute to the appearance of ring 1. Those results reveal that our 200 °C DLE-CVD Co film is a mixed phase of fcc-Co and hcp-Co, which is in accordance with our previous report.[39] When higher deposition temperatures are applied, only fcc-Co phase is observed. We hypothesize that the competing growth between hcp-Co (low-temperature phase) and fcc-Co (high-temperature phase) induced lattice frustration and suppressed the growth of larger crystals, producing nanocrystalline films, which are favorable for Cu liner/capping applications.[100-101]

Table 3.2. Theoretical and experimental lattice parameters for a 200 ℃ DLE-CVD Co film from TEM electron diffraction results. The indices of planes (hkl) and interplanar spacings (d) are from the reference crystal structures of fcc-Co (JCPDS Card No.15-0806), hcp α-Co (JCPDS Card No. 71-4239).

	Theoretical value				Experimental value		
	FCC β-Co		Hcp α- Co		Temperature = 200 ℃		
No.	hkl	d(A)	hkl	d(A)	Ring no.	Calculated d (A)	error
1	111	2.05	002	2.03	1	2.0679	0.87%
2			101	1.92	2	1.9071	-0.67%
3			102	1.48	3	1.5307	3.43%
4	220	1.25			4	1.2636	1.09%
5	311	1.07			5	1.0998	2.79%

Table 3.3. Theoretical and experimental lattice parameters for a 230 ℃ DLE-CVD Co film from TEM electron diffraction results. The indices of planes (hkl) and interplanar spacings (d) are from the reference crystal structures of fcc-Co (JCPDS Card No.15-0806)

	Theoretical value		Experimental value		
	FCC β-Co		Temperature = 230 ℃		
No.	hkl	d(A)	Ring no.	Calculated d (A)	error
1	111	2.05	1	2.0523	0.11%
2	200	1.77	2	1.7884	1.04%
3	220	1.25	3	1.255	0.40%
4	311	1.07	4	1.0676	-0.22%

Table 3.4. Theoretical and experimental lattice parameters for a 260 °C DLE-CVD Co film from TEM electron diffraction results. The indices of planes (hkl) and interplanar spacings (d) are from the reference crystal structures of fcc-Co (JCPDS Card No.15-0806)

| | Theoretical value | | Experimental value | | |
| | FCC β-Co | | Temperature = 260 °C | | |
No.	hkl	d(A)	Ring no.	Calculated d (A)	error
1	111	2.05	1	2.0523	0.11%
2	200	1.77	2	1.8355	3.7%
3	220	1.25	3	1.259	0.72%
4	311	1.07	4	1.0863	1.52%

3.4   Evaluation of DLE-CVD Co as Liner Material for Cu Interconnects

3.4.1   Co Liner Against Cu Diffusion

Based on the Co-Cu phase diagram, Co and Cu do not diffuse into each other at temperatures below 700 K, and only partially intermix at temperatures up to 1000 K from the thermodynamic point of view.[102] With high conformality, uniformity and smoothness, our nanocrystalline Co films have appropriate properties to be used as an effective copper barrier and capping layer for Cu interconnects in microelectronics.[92, 103] In order to evaluate the copper barrier performance of our DLE-CVD Co, capacitance-voltage (C-V) characteristics of Cu/Co/SiO$_2$/Si and Cu/SiO$_2$/Si systems were studied both before and after annealing at 600 °C. Fabrication details of the micro-capacitors are described in the experimental section.
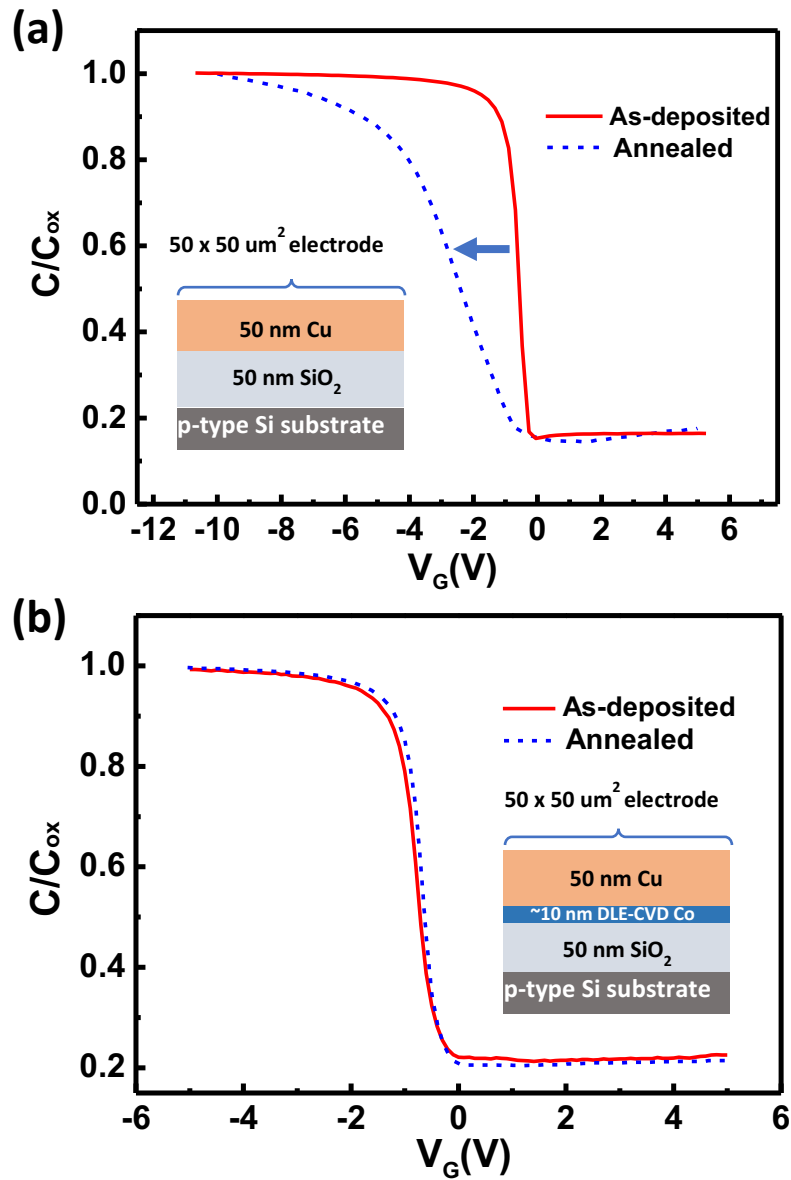
Figure 3.11. C-V measurements on microcapacitor structures for the evaluation of Cu blocking capability. (a) Cu/SiO$_2$/Si system, showing ~2 V shift to the negative side; (b) Cu/Co/SiO$_2$/Si system, showing no observable shift of C-V curve. All measurements started at positive 5 V and scanned from positive bias toward negative bias.

Figure 3.11(a) presents the C-V curve of the Cu/SiO$_2$/Si system without any capping

layer or liner, which shows a roughly 2 V shift toward the negative region after

annealing. This phenomenon indicates that Cu ions diffused into the SiO$_2$ layer and

formed positive charges.[83] However, as shown in Figure 3.11(b), the Cu/Co/SiO$_2$/Si

system presented no observable shift of C-V curve, indicating that Cu is effectively

prevented from diffusing into SiO$_2$ by DLE-CVD Co at up to 600 °C. Since Co has much

higher conductivity (1.60 × 10^7 S/m) than most metal nitrides, e.g., TaN (0.76 × 10^6 S/m),

the application of a Co liner may decrease the thickness of the barrier required for

blocking Cu diffusion, while maintaining a low overall conductivity as close to pure Cu

(5.96 × 10^7 S/m) as possible.[11, 82, 104] In this sense, the application of Co can potentially

decrease energy consumption during electron transport in Cu interconnects.[89]

Moreover, the strong adhesion at the Co/Cu interface can also substantially suppress

surface electromigrations in Cu interconnects, thus increasing the lifetime of

microelectronics devices.[105]

3.4.2 All-Around Encapsulation of Nano-Scale Cu Wire with DLE-CVD Co

Taking advantage of the Cu barrier performance, smooth nanocrystallinity and Cu

surface adhesion of DLE-CVD Co, here we demonstrate that a nanocrystalline DLE-CVD

Co film is an effective liner/capping material to three-dimensionally encapsulate Cu

interconnects, thus enhancing their thermal stability and also suppressing potential

electromigration. As a testing platform, nanoscale Cu wires were encapsulated all-around by DLE-CVD Co on thermal oxide substrates. In detail, a 10 nm thick Co film is first deposited onto a thermal oxide substrate, then 500 nm wide Cu lines with a thickness of 60 nm were deposited onto the Co surface by standard e-beam lithography, metallization and lift-off processes. Afterwards, a final Co layer was deposited onto the Cu surface by DLE-CVD. In this case, the bottom Co layer is serving as liner material, top Co layer is serving as capping layer, thus the Cu wire is thoroughly encapsulated by DLE-CVD Co. Meanwhile, as a control sample, bare Cu wires with no Co encapsulation layer were also deposited onto a thermal oxide substrate by the same method.

Figure 3.12 (a-b) shows cross-section EDAX elemental mapping and SEM image of a Co-encapsulated Cu wire, demonstrating that the Co film is uniformly coated all around the Cu wire. After annealing at 600 °C for 2 hours, the EDAX elemental mapping images in Figure 3.12 (c-d) show that the Cu distribution is mostly maintained for the Cu wire sample encapsulated by DLE-CVD Co. However, as a control experiment, Figure 3.12 (e-f) indicate that a substantial amount of Cu diffused into SiO_2 when Co encapsulation is not applied around a Cu wire, since many more EDAX Cu counts were detected within the SiO_2 layer after annealing. This demonstration provides direct evidence that DLE-CVD Co nanocrystalline films are suitable as liner/capping layers that can substantially increase the reliability and lifetime of nanoscale Cu interconnects.
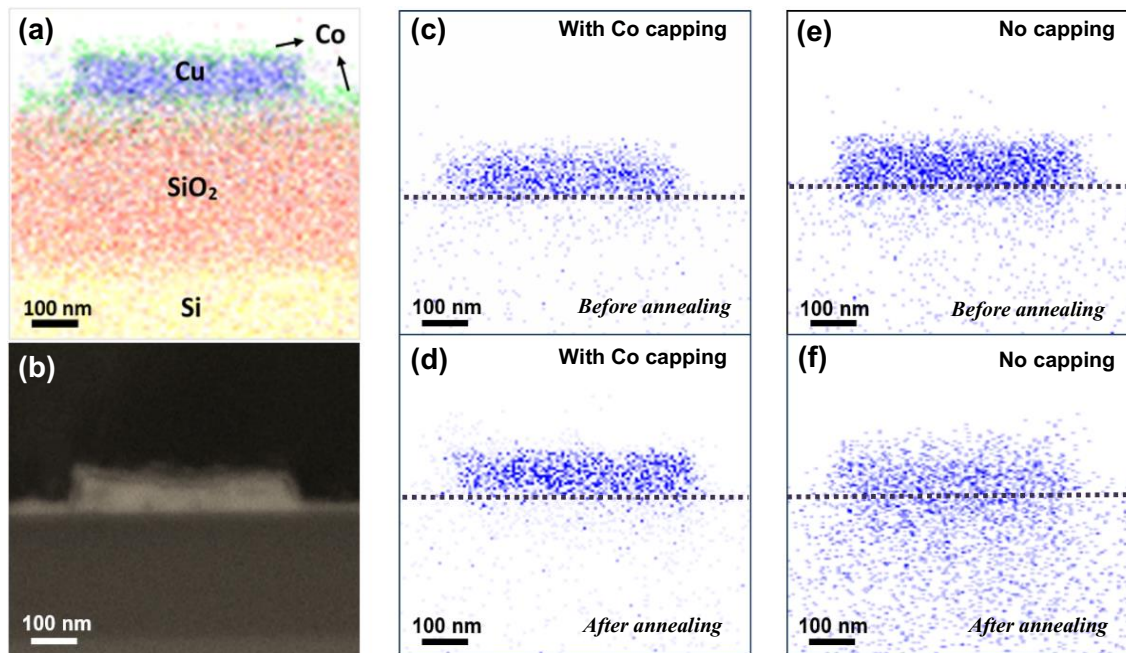
Figure 3.12. Demonstration of the application of DLE-CVD Co as an all-around encapsulation layer for Cu interconnects at nanoscales. (a) Cross-section EDAX elemental mapping of a Co-encapsulated Cu wire; (b) Cross-section SEM image of a Co-encapsulated Cu wire; (c-d) Cross-section Cu Kα1 2D mapping of the Cu wires with Co encapsulation before and after annealing at 600 °C for 2 hours, showing no obvious diffusion of Cu; (e-f) Cross-section Cu Kα1 2D mapping of the Cu wires without any capping layer before and after annealing at 600 °C for 2 hours, showing substantial amount of Cu diffusion into SiO_2.

3.5   Conclusions

In this chapter, we demonstrated that DLE-CVD Co with highly controllable growth

characteristics is a promising liner/capping layer for nanoscale Cu interconnects.

Microscopic and crystallographic studies show that our DLE-CVD Co is composed of

highly smooth nano-crystallines with a grain size of ~10 nm and surface roughness rms

of ~0.9 nm. Less than 0.8 at% of impurities were observed in APT analysis results for

films deposited at 200 ^{o}C. Based on the nanoscale analysis of samples with and without

Co encapsulation, it is proved that the diffusion of Cu is effectively blocked by DLE-CVD

Co. Finally, with a nanoscale Cu line encapsulated all-around by Co as a proof-of-concept

model, we demonstrate that our DLE-CVD Co encapsulation layer is able to substantially

improve the thermal stability of nanoscale Cu interconnects. Also, taking advantage of

the high conductivity and lower carrier MFP of Co, DLE-CVD Co encapsulation layers can

potentially further decrease the power consumption of Cu interconnects with

dimensions smaller than the MFP of Cu. This approach could allow the fabrication of Cu

interconnects with higher efficiency in future microelectronic devices.

Chapter 4   Atom Probe Tomography (APT) Analysis of DLE-CVD Metals

4.1   Introduction

Optical microscopes enabled the observation of physical phenomenons at micrometer scales, while more advanced imaging techniques including scanning electron microscopy (SEM), transmission electron microscope (TEM) and scanning probe microscopy (SPM) have enabled the investigation of materials at nanometer scales.[106] The development of semiconductor electronics in the past decade have introduced new challenges to material science, bringing the need to study materials at atomic level.[107] Atom probe tomography (APT) is an advanced characterization technique with ultra-high atomic resolution for both composition and morphology.
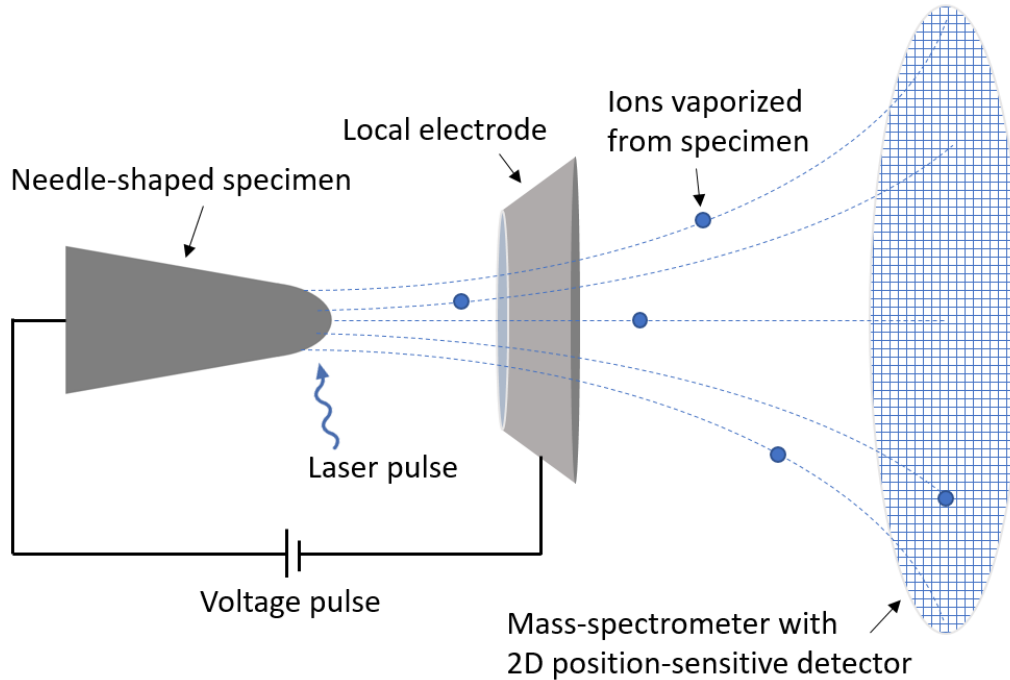

Figure 4.1. Diagram of an atom probe tomography (APT)

The diagram of an APT is illustrated in Figure 4.1. During an APT analysis, individual atoms are electrically evaporated and ionized one by one from the surface of a needle-shaped specimen by a certain kind of excitation, and analyzed by a mass spectrometer with 2D position-sensitive detector to obtain their chemical and positional information at the same time.[108] With regard to excitation sources, a voltage pulse is required to pull the evaporated ions toward the local electrode, which is called a "field evaporation" process.[26] However, the use of very-high-voltage pulses introduces many disadvantages, including a large energy spread of the evaporated ions that reduces resolution, and a high mechanical stress at specimen apex that makes the sample to fracture easily.[109] To solve this problem, laser-assisted APT was developed. In laser-assisted APT, a pulsed laser is used in addition to the pulsed voltage excitation. With proper synergy between the laser pulse and voltage pulse, a much lower bias between the specimen and the local electrode is required, thus substantially reducing energy spread and mechanical stress on the specimen, increasing resolution and analysis reliability.[110]

For metallic materials, especially high-purity metal, APT technique offers many advantages over other characterization techniques, because it can obtain the information about trace amount of impurities, grain boundaries, depth profile, and isotope composition all at the same time. Moreover, the specimen required for APT is only a needle at 100-nanometer scale, which is highly favorable when it is difficult or expensive to obtain large-quantity samples for other chemical analysis. However, since a

specific shape of specimen is critical for APT analysis, sample preparation processes are

highly challenging and usually need to be separated developed for different materials in

different scenarios.

In this chapter, APT technique is used to study the chemical composition of cobalt,

nickel, and nickel silicide thin films. The sample preparation processes for different

materials in different structures are described. APT parameters and final APT results are

also thoroughly discussed.

4.2 APT of DLE-CVD Cobalt Metal for Compositional Studies
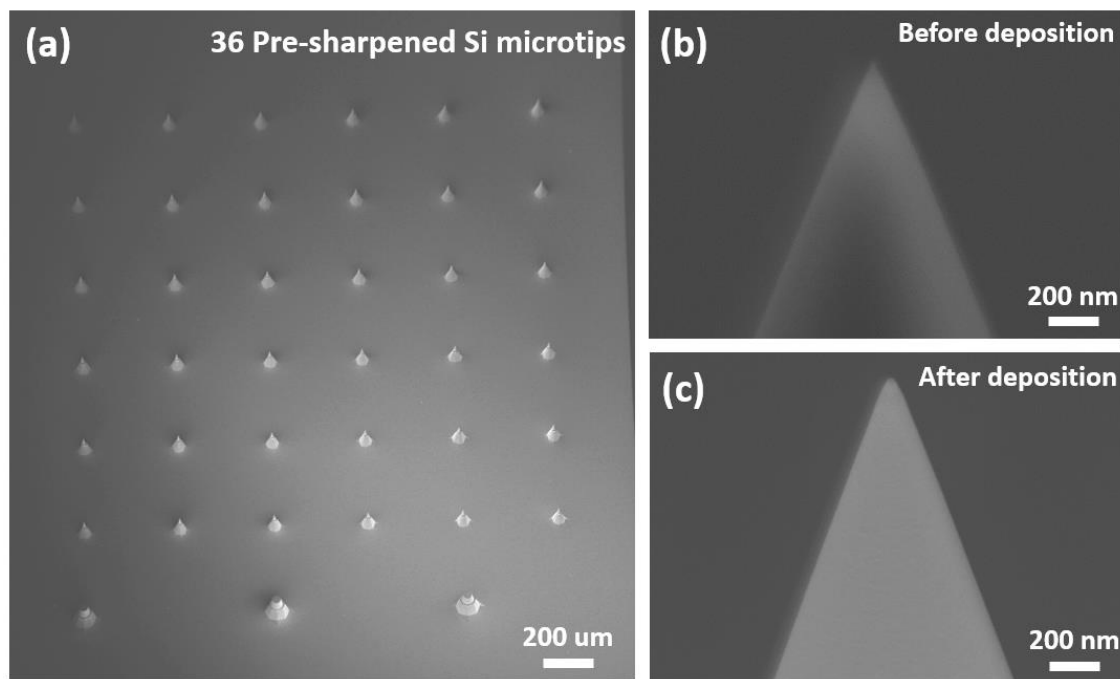
Figure 4.2. (a) SEM image of a coupon with 36 pre-sharpened silicon micro-tips (PSM);

(b) A magnified SEM image of a PSM before DLE-CVD Co coating; (c) A magnified SEM

image of a PSM after DLE-CVD Co coating.

Since our DLE-CVD process produces high-purity cobalt thin films (discussed in Chapter 2), APT analysis is needed to detect the trace amount of impurities and to study the impurity distribution in the film. We started the APT sample preparation by coating DLE-CVD Co films with precisely controlled thickness on an array of silicon microtips pre-sharpened to less than a 10-nm tip radius and 10° shank angle, the SEM image of the microtip array is shown in Figure 4.2(a). 25 nm of Co films by different deposition conditions were deposited onto the pre-sharpened silicon microtips (PSMs). After DLE-CVD cobalt coating, highly smooth and conformal Co films are observed on the microtips, as is demonstrated in Figure 4.2(c). The final needle-shaped specimens with DLE-CVD cobalt coating have tip radius between 50 nm and 70 nm, and with shank angles around 10°.

Figure 4.3. (a) 3D atomic reconstruction of the 200 ^{o}C DLE-CVD specimen, in which blue dots are Co (0.5 % of all Co atoms displayed), grey dots are Si (50 % displayed), green

dots are O (100 % displayed), orange dots are C (100 % displayed), and red dots are N (100 % displayed). (b and c) Silicon and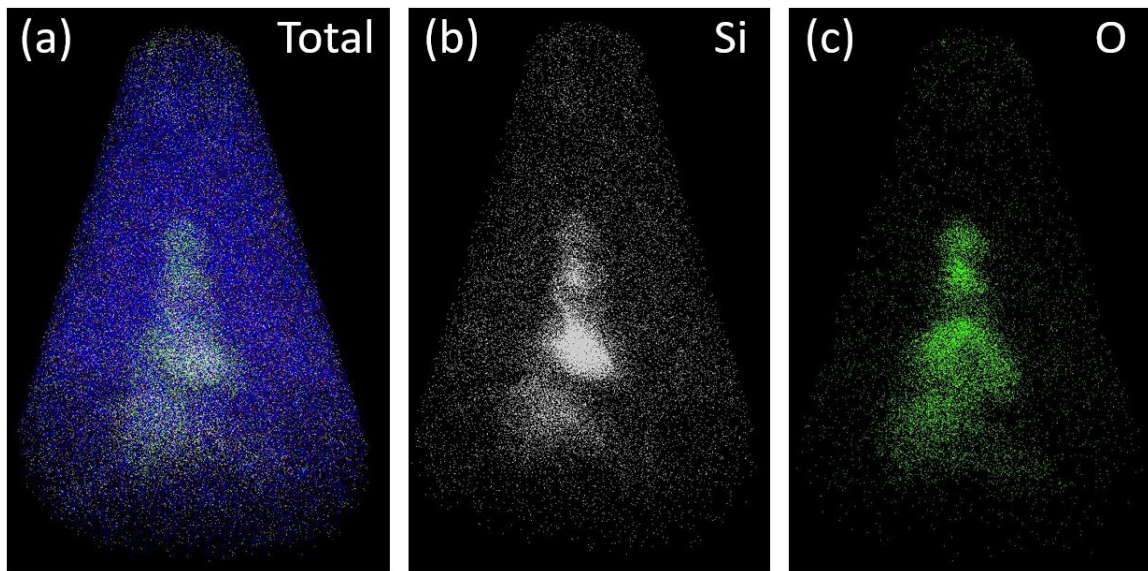 oxygen signal, showing the distribution of oxygen is mostly at the silicon/cobalt interface, rather than in the bulk of cobalt.

Laser-assisted APT analysis is then performed on the coated microtips at 40 K under a vacuum pressure lower than 5×10^{-11} Torr. A 532 nm laser with 50 pJ pulse energy was used to assist ion evaporation at a pulse frequency of 100 kHz. Data reconstruction was performed with IVAS software (Cameca, Gennevilliers, France), extracting three-dimensional quantitative compositional and structural information.[111] Figure 4.3 shows the reconstructed 3D atomic distribution of the 200 °C DLE-CVD Co film, in which the blue-colored dots are cobalt, green dots are oxygen and grey dots are silicon. No substantial clustering or accumulation of impurities is observed in the bulk of the sample, and the majority of oxygen atoms exist at the silicon/cobalt interface, which is due to the UV-Ozone cleaning performed before DLE-CVD deposition in order to completely remove organic residues left from the lithography processes.

Table 4.1. Compositional data of DLE-CVD Co acquired from APT

at%	Co	C	N	O
200 °C	98.00 ± 0.20	0.76 ± 0.38	0.53 ± 0.28	0.71 ± 0.25
230 °C	96.80 ± 0.30	1.80 ± 0.35	0.33 ± 0.18	1.07 ± 0.30

In Table 4.1, compositional data are collected from only the film part, excluding the atoms from the silicon tip and its surface. The sample deposited at 200 °C shows less than 0.8 at% of each contaminant (C, N and O), and the sample deposited at 230 °C contains less than 1.8 at% of these impurities. In APT reconstruction data, mild oxidation at the surface of cobalt thin film were observed, which we believe is due to air exposure after taking samples out of the deposition chamber for APT analysis. Therefore, in order to obtain bulk composition data, we excluded the ions emitted from specimen surface by manually excluding the initial ions detected, as illustrated in Figure 4.4.
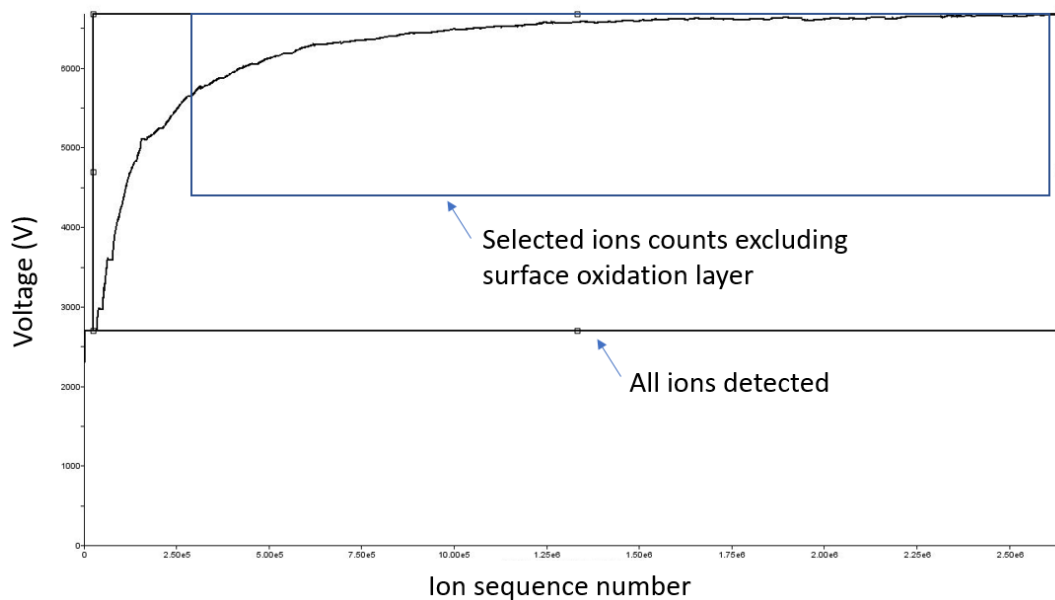
Figure 4.4. Voltage history of an APT experiment on 200 °C DLE-CVD cobalt. The larger box denotes all ions detected during the analysis; the smaller box denotes the signals selected for bulk composition study without being impacted by surface oxidation.

With regard to the sample preparation method, the above mentioned PSM method offer the advantage of convenience, standardization and high efficiency. Nevertheless, in some cases, films can only be deposited onto a specific substrate without pre-sharpened tips. In these cases, a general focused ion beam (FIB) milling process can be used to obtain specimens and sharpen them into the required needle shape with tip radius smaller than 100 nm. Here we use DLE-CVD Co deposited onto a flat-top Si substrate as an example to demonstrate how a universal sample shall be acquired.

Figure 4.5. A universal focused ion beam (FIB) milling process to acquire APT specimen from any substrate. (a) Attached a small piece of coated substrate onto a metal grid; (b) Use rectangular milling to cut a smaller piece out of the sample; (c) Use annular milling to make a <300 nm needle; (d) Use fine milling to sharpen the specimen into <50 nm tip.

As shown in Figure 4.5, DLE-CVD Co was first coated onto a Mo metal substrate, then a small piece of the coated substrate was attached to a metal grid for easier handling with FIB soldering. Rectangular milling around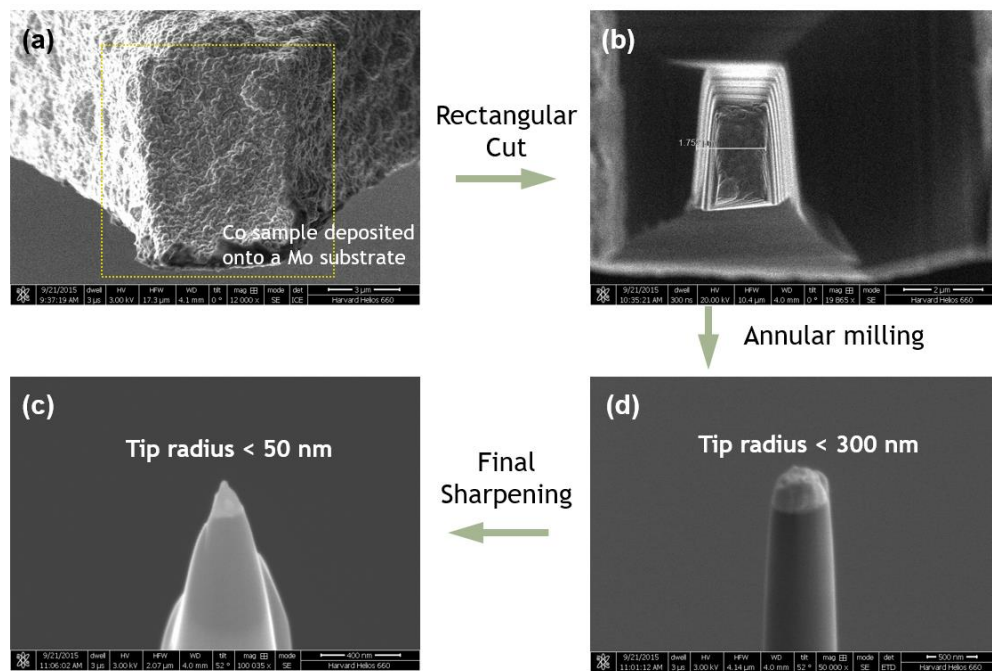 the center of the sample piece was conducted to make a smaller-size specimen, in order to apply annular milling process to make <300 nm needles. The last step is fine annular milling to sharpen the specimen into the final <50 nm tips for APT analysis.

4.3   APT of Ni and NiSi from Deep Inside of High-Aspect-Ratio Trenches

4.3.1   Ni and NiSi Sample Acquisition from Deep Trench Structures

Previously, we developed DLE-CVD processes for nickel and nickel silicide as is presented in recent reports from our group.[41-42] We demonstrated highly conformal DLE-CVD Ni metal deposited onto a 10:1 aspect ratio trench structure, as shown in Figure 4.6.[112] Ni thin film thicknesses were measured to be the same on both inside and outside of trench test structures, proving its conformal growth characteristics. Moreover, as the film grows thicker, the aspect ratio of the resulting trench increases from 10:1 up to 40:1 near the end of the deposition. This indicates that the DLE-CVD process offers highly conformal and uniform Ni thin films up to 40:1 aspect ratio. One of the application of Ni metal is local interconnect to form ohmic contact with silicon, because Ni can form low-barrier $NiSi_x$ upon proper annealing at Si/Ni interface.[113]
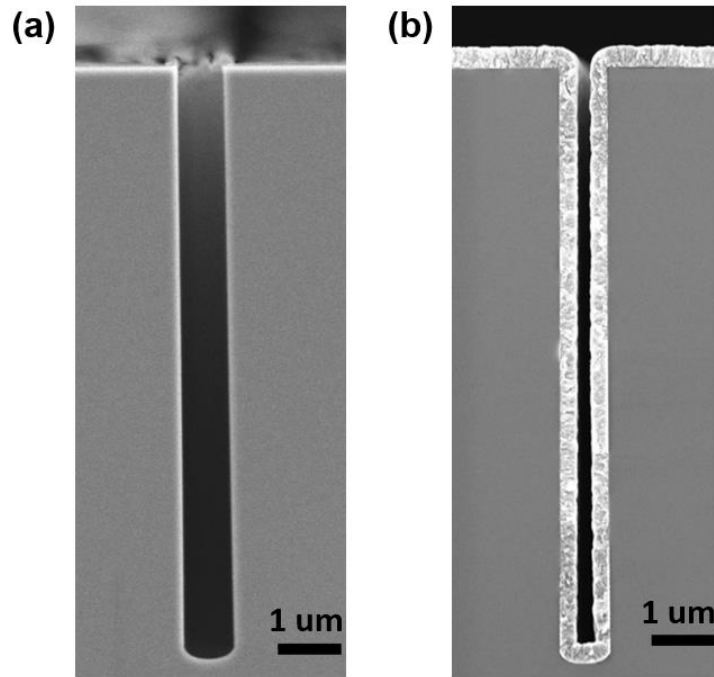
Figure 4.6. (a) A 10:1 aspect-ratio trench test structure; (b) Ni metal coated trench, demonstrating the conformality and uniformity of the DLE-CVD Ni film.[112]

Although DLE-CVD process offers high conformality, it is possible that some properties of the material deposited inside will be different from the material deposited outside of complex structures like trenches and holes.[32] For example, due to the limit of kinetic diffusivity of precursors under vacuum, precursor vapor concentrations may be different at inside and outside of high-aspect-ratio structures during deposition, thus causing different chemical compositions at different depths of a trench. Unfortunately, previous characterizations of these materials were performed on planar substrates rather than on the specimens from inside of complex structures, which could not

provide evidence to either prove or deny the above-mentioned possibility of inside/outside difference.[114]

To obtain high-resolution compositional and structural characterization data, APT only requires a nanometer-scale specimen, which is a favorable analysis method when it comes to the examination of extremely small local areas of a sample. Meanwhile, FIB lift-out fabrication technique offers the practical method to retrieve sample pieces from inside parts of complex structures, and cut them into needle shapes with <50 nm apex diameter.[115] In this regard, the combination of FIB and APT provide the feasibility of directly analyzing specimens from inside of complex structures with atomic resolution, which is a strategy to test the uniformity throughout different parts of a high-aspect-ratio structure.

Here in this section, we demonstrate a FIB/APT process to study the inside/outside difference of conformal thin films in complex structures, using our previously reported DLE-CVD Ni and the NiSi$_x$ formed at Ni/Si interface as two examples. The FIB lift-out process is schematically illustrated in Figure 4.7. After deposition onto trench test structures, one side of a trench (black dashed box in Figure 4.7b), is lifted out. Silicon posts (serve as sample holders) with flat tops are then welded onto different parts of the sample chunk. As shown in Figure 4.7(c), the outside part of the sample is welded to Pole A, and the inside part is welded to Pole B. Afterwards, the sample chunk is cut into two smaller pieces as illustrated with dashed lines in Figure 4.7(c).
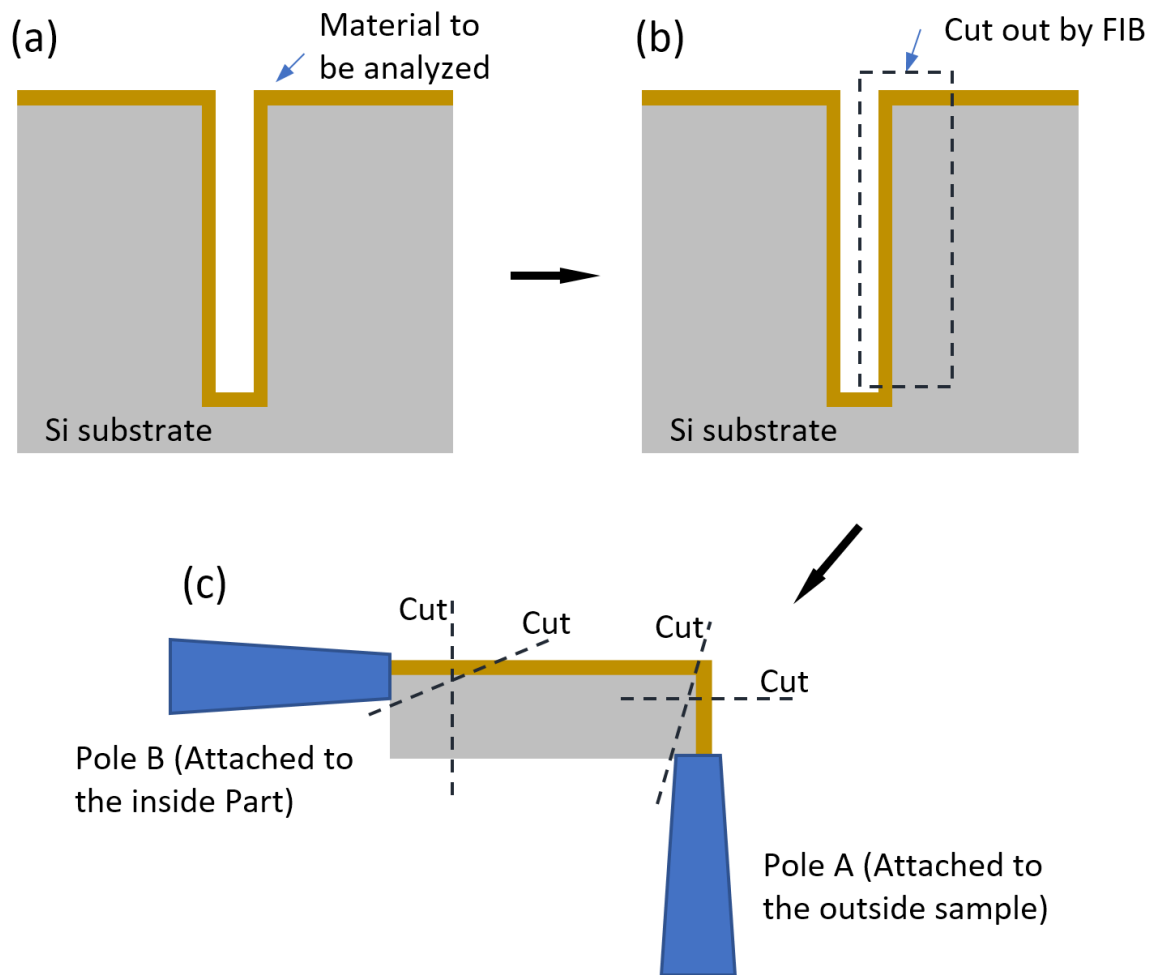
Figure 4.7. Schematic illustration of focused ion beam (FIB) lift-off technique. (a) Cross-section of a trench coated with the thin film material to be analyzed; (b) FIB sectioning of a target region, which contains both the inside and outside part of the sample; (c) The lifted-out sample chunk is then welded with two Si poles at different positions.

After obtaining the inside and outside thin film specimens on Pole A and Pole B, we then conducted rough cutting and annular milling on these two specimens to finalize the

APT sample preparation. Figure 4.8 shows the SEM images at different stages of the sharpening and milling processes. Before these processes, we deposited 100 ~ 200 nm of amorphous carbon to protect the samples from potential damages by Ga^+ ion beam. Eventually, the specimens are sharpened into small needles with apex diameter less than 20 nm, which are ready for APT analysis. Same FIB sample preparation processes were conducted on both Ni and NiSi samples.
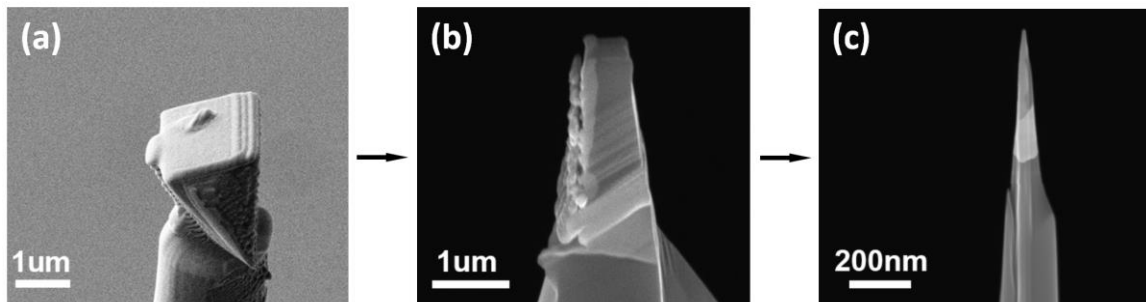
Figure 4.8. (a) SEM of a specimen welded onto a Si pole; (b) After rough sharpening into pyramid shape; (c) After fine annular milling into needle shape.

4.3.2   APT Parameters and Reconstruction Results of Ni and NiSi

APT results of both inside and outside specimens for Ni thin films are shown in Figure 4.9, and the same results for $NiSi_x$ are shown in Figure 4.10. Roughly 40×30×200 nm^3 analyzed volume for all 4 samples can provide large statistical dataset, thus ensuring high analysis resolution and reliability. Figure 4.9 b,e, c,f and Figure 4.10 b, d are the spatial reconstruction results plotted by projecting detect atoms into 3D graphs. Si and Ni atoms are denoted by grey and blue dots, respectively.
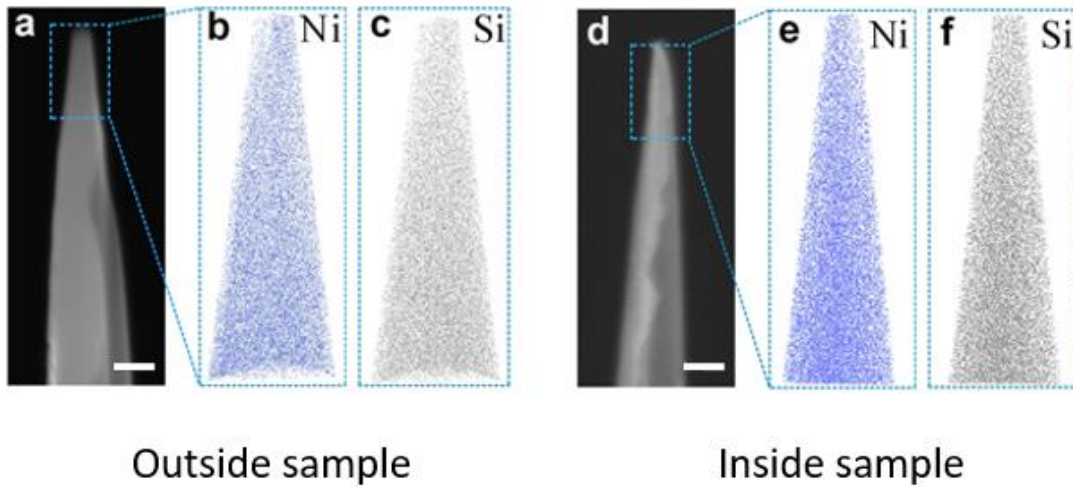
Figure 4.9. Elemental APT reconstruction images of the NiSi$_x$ specimens acquired from outside (b-c) and deep inside (e-f) of a trench, corresponding with the SEM images shown in (a) and (b), respectively. Scale bars denote 100 nm.
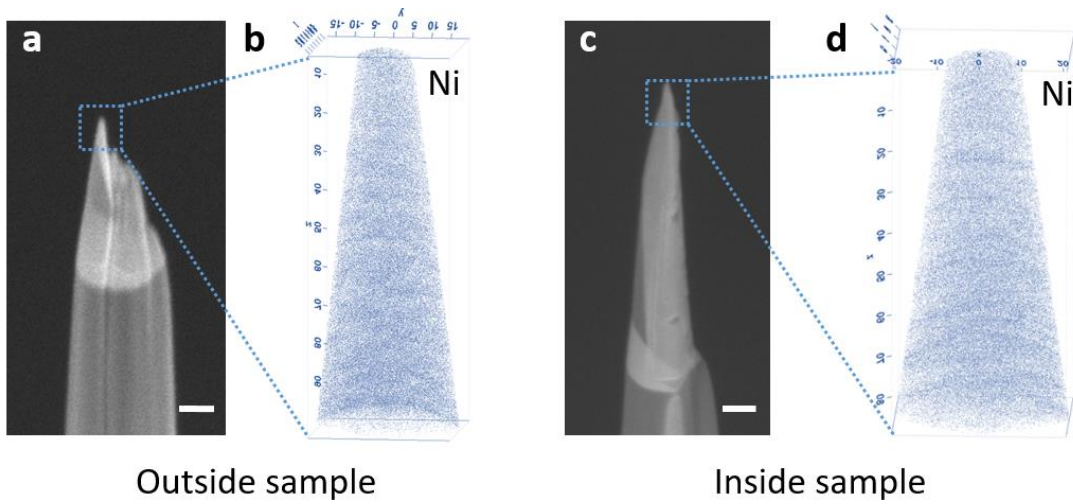
Figure 4.10. Elemental APT reconstruction images of the Ni specimens acquired from outside (b) and deep inside (d) of a trench, corresponding with the SEM images shown in (a) and (b), respectively. Scale bars denote 100 nm.

The atom distribution in all 4 samples show no observable phase segregation or clustering phenomenon. The results indicate that our DLE-CVD process create highly uniform Ni films, and the NiSi$_x$ thin film converted from DLE-CVD Ni is a single-phased material with uniform Ni to Si ratio in the bulk of the film.
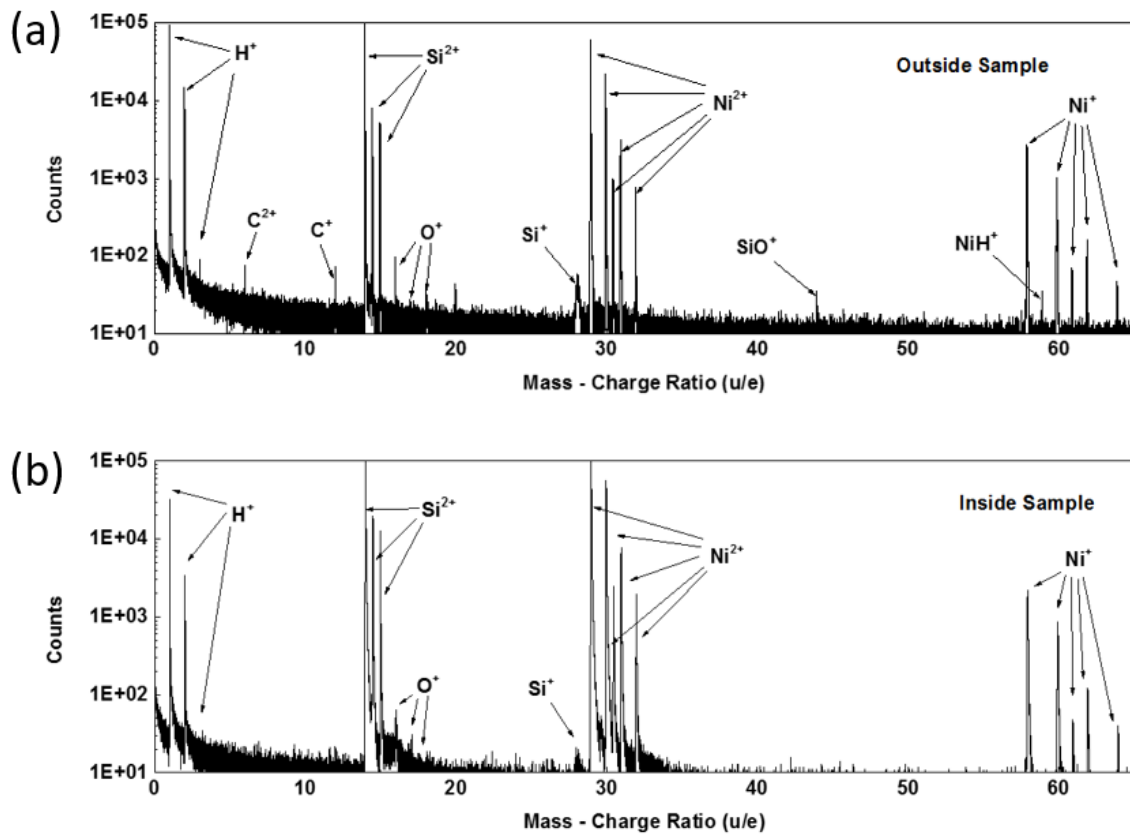
Figure 4.11. Original mass spectrum of NiSi specimens obtained outside (a) and inside (b) of trench structures. All peaks with over 50 counts are labeled in the figures.

For the study of NiSi$_x$ at this point, we can only draw the conclusion that we have a single-phased nickel silicide, but the exact type of silicide (i.e. Ni to Si ratio) is yet to be

identified for both the inside and outside NiSi$_x$ samples. For this information,

quantitative study of NiSi$_x$ composition was performed by statistically analyzing the

original mass spectra (Figure 4.11). The analyzed data is from a cylindrical region with

diameter of 10 nm. During the APT data processing, data points from the surfaces of

both specimens are intentionally omitted, so that we can avoid including the surface

areas contaminated during the sample preparation procedures (Figure 4.12). Nearly 1:1

concentrations of Ni and Si atoms are observed in the composition data, and the atom

distributions are highly uniform for both Ni and Si. Based on these results, it can be

concluded that the analyzed specimen is a single phase of nickel monosilicide (NiSi),

instead of nickel disilicide (NiSi$_2$) or a mixture of various phases.
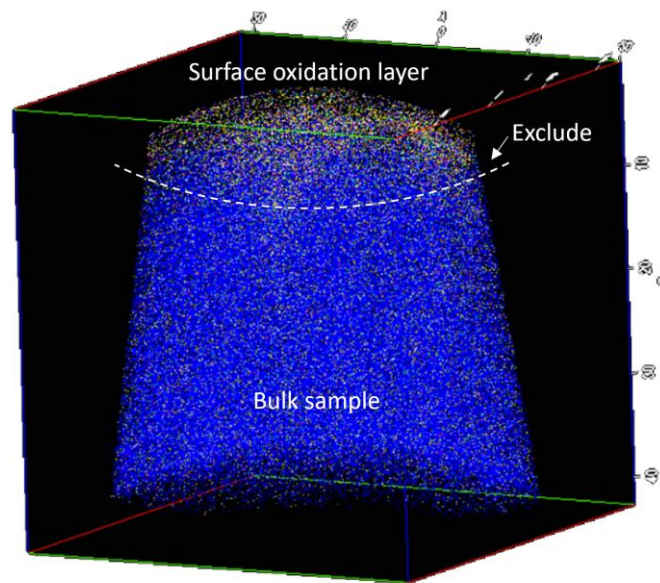
Figure 4.12. Illustration of the exclusion of surface regions in data analysis process. The

surface contamination may due to air exposure after taking the sample out of

deposition chamber, or may due to the damage happened during sample preparations.

As summarized in Table 4.1, quantitative elemental composition data is calculated with IVAS software (Cameca, Gennevilliers, France). In our DLE-CVD Ni thin film, about 4 % nitrogen was detected, which is favored for the formation of highly smooth NiSi thin films at Ni/Si interface as discussed in previous reports.[116] While in the NiSi sample, the detected O, N and C impurities were roughly 0.05 % combined, demonstrating that super-high-purity NiSi is formed by the silicidation of DLE-CVD Ni metal.

Table 4.2. Quantitative compositional information of NiSi and Ni samples acquired from both outside and inside of trench structures.

NiSi sample	Outside Trench	Inside Trench
Element	Atomic Percentage (%)	Atomic Percentage (%)
Ni	52.00 ± 0.03	50.12 ± 0.05
Si	47.87 ± 0.10	49.83 ± 0.09
C	0.02 ± 0.01	0.005 ± 0.004
N	0.04 ± 0.02	0.03 ± 0.02
O	0.07 ± 0.03	0.015 ± 0.005

Ni sample	Outside Trench	Inside Trench
Element	Atomic Percentage (%)	Atomic Percentage (%)
Ni	93.42 ± 0.10	94.98 ± 0.10
Si	not detected	not detected
C	1.52 ± 0.15	0.95 ± 0.20
N	4.09 ± 0.10	3.66 ± 0.09
O	0.97 ± 0.30	0.41 ± 0.20

Compared with the composition of the as-deposited Ni film, the N, O and C impurity levels dramatically decreased after the silicidation process. These impurities did not diffuse into the silicon along with nickel, and thus they remain in the unreacted nickel, which will be eventually etched away from the surface. We note that these ultra-low impurities contents in NiSi are very difficult to detect or undetectable by most conventional elemental analysis methods like XPS, RBS and EDX. In this regard, APT enables the quantitative analysis and visualization of trace amounts of impurities at atomic resolution, which provides the guideline for the application of advanced functional materials in future semiconductor devices.

4.4   Conclusions

In this chapter, cobalt, nickel, and nickel silicide thin films are studied with APT technique. To analyze samples in different structures, specific sample preparation methods and processes are discussed, including pre-sharpened microtip (PSM) method and FIB milling processes. A FIB lift-out process to acquire specimens from deep inside of a high-aspect-ratio trench structure is also demonstrated with DLE-CVD Ni and the NiSi converted from DLE-CVD Ni. From the APT results, both compositional and structural information were obtained. These works provide general experimental guidelines for APT analysis on metallic thin film materials, especially for high-purity metals in high-aspect-ratio structures, which are crucial components of the interconnect architectures in advanced semiconductor devices.

Chapter 5   Surface Metallization of Polymer Fibers for Flexible Electronics

5.1   Introduction

Metal interconnects in the traditional semiconductor industry enable communication among active units (e.g. transistors, sensors and actuators) in electronic devices. For flexible electronics, interconnects are also needed for the same reason.[117-118] In addition to the traditional requirements for metal interconnects, flexible electronics further requires mechanical flexibility and durability, which is highly challenging since thin metal wires tend to be fragile.[119] Direct metallization onto the surface of polymer fibers is one potential method to fabricate flexible conductive interconnects, which offers the flexibility and strength of a fiber core and the conductivity of a metal shell at the same time.[54, 59]

Thin fibers in bundles tend to pack closely with each other, which is equivalent to a complex structures with ultrahigh aspect ratios. Therefore, a highly conformal thin film deposition technique that can coat deep inside of a high-aspect-ratio structure is needed to effectively metallize fiber bundles. Furthermore, to obtain uniform coating for all fibers in a bundle, the deposition method needs to provide saturated film growth at both outer and inner parts of the bundle.

Besides the conformality requirements on the deposition method for fiber surface metallization, high metal nucleation density and strong interfacial adhesion between

metal and polymer are also critical prerequisites for successful fabrication of flexible conductive fibers. Thus, proper surface modifications and treatments may be necessary before metal deposition to create active functional groups for nucleation, or to provide strong chemical bonding between the polymer core and deposited metal.

5.2 Advantage of DLE-CVD for the Surface Metallization of Polymer Fibers

Direct-liquid-evaporation chemical vapor deposition (DLE-CVD) is a novel CVD method developed in recent years, which substantially improves conformality of metal depositions and offers depositions at relatively low temperatures.[42, 96] Precursor delivery rates of DLE-CVD are not limited by precursor vapor pressures like traditional CVD is. Therefore, precursors in DLE-CVD deposition chamber can reach much higher gas-phase concentrations and saturate all surfaces in complex structures, minimizing the growth rates difference at positions with different aspect-ratios.[41] Furthermore, when thicker coating or some specific metal coating is needed, a relatively thin conformal coating produced by DLE-CVD can serve as a seed layer for additional metallization by electroplating, which is an established strategy for interconnect fabrication in the traditional silicon semiconductor industry. Polymer fibers tend to form dense bundles, which are essentially high-aspect-ratio structures. In this sense, DLE-CVD have great advantage in coating fiber bundles because of the super-high conformality it offers. However, practical application of DLE-CVD processes for polymer fiber metallization has not yet been demonstrated.

In this chapter, we introduce the use of DLE-CVD to effectively metallize polyaramid fibers, including Kevlar and Nomex. Taking advantage of the high precursor vapor pressure offered by DLE-CVD, highly uniform and conformal metal thin film can be deposited onto single polyaramid fibers or bundles of them. With a series of surface pretreatments, we achieved high nucleation density that fully covers all fiber surface, and achieved well-adhered metal-polymer interface without observable delamination after cross-sectioning with FIB. Detailed characterization results and potential applications of the coated fibers are presented and discussed. The results show that DLE-CVD is a highly promising technique to fabricate polymer fiber bundles into conductive and flexible building blocks in flexible electronics.
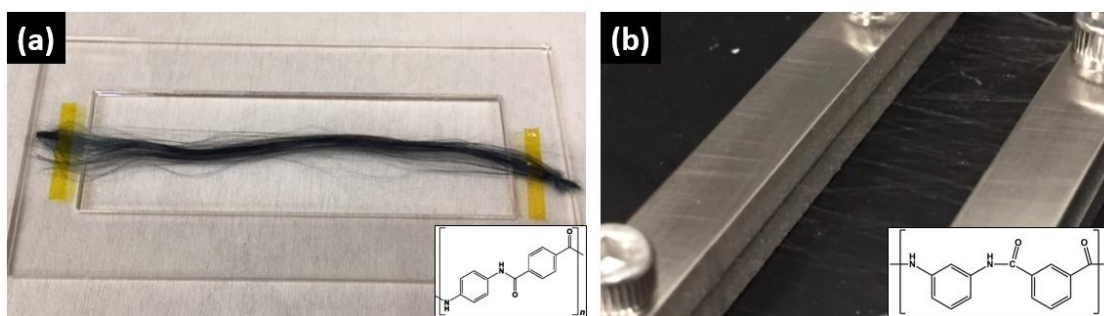

Figure 5.1. (a) A bundle of Kevlar fibers taped onto a plastic sample holder; (b) Nomex fibers laterally electrospun onto a metal sample holder. Insets are the chemical structures of Kevlar and Nomex polymers.

5.3   Experimental Details

Kevlar fibers (⌀11 um, black) used in this work was obtained from The Thread Exchange,

Inc. For easier handling during the experiments, Kevlar fibers are taped on plastic or

metal sample holders as shown in Figure 5.1(a). Nomex fibers were prepared with an in-

house electrospinning apparatus made by IME Technologies, using Nomex polymer

(Sigma Aldrich) dissolved in dimethylacetamide (DMAc) as the precursor.[120] Nomex

fibers with 100~300 nm diameters were made and transferred onto metal sample

holders as shown in Figure 5.1(b).

DLE-CVD of Co was performed with a tube-furnace CVD reactor equipped with DLE

delivery system, which is the same system described previously in the Figure 3.3 of

chapter 3. The default deposition condition was set at 200 $^\circ$C with 100 sccm H_2 and 100

sccm NH_3 co-reactant gases.

SEM images were taken by a Zeiss FE-SEM Ultra55 with inlens detector. FIB cross-

section imaging was performed on a FEI Helios 660 system. Electroplating of copper

onto the DLE-CVD Co seeded fibers was done on a home-built electrochemical setup,

with Keithley 2400 sourcemeter and a pure copper anode.

5.4   DLE-CVD Metallization on Kevlar Fibers and Its Challenges

Polyaramid is a category of high-performance synthetic fibers first developed by DuPont

in early 1960s.[121] Polyaramid fibers offer the benefits of lightweight, heat resistance and

high mechanical strength, which made them widely used in composite materials for body armors, airplane frames, high-performance automobile tires, etc.[122]

For the application of Kevlar fibers as interconnects in flexible electronic devices, an effective surface metallization method is needed. Since Kevlar fibers are thermally stable up to 482 °C (data from "Kevlar Technical Guide" by DuPont), it is practical to use heated gas-phase thin film deposition methods, including CVD, for the metallization of Kevlar. CVD process requires sufficient nucleation sites, e.g. hydroxide groups or amine groups, on sample surface, however, commercial polymer fibers usually have an inert surface. Therefore, proper surface cleaning and modification are necessary to effectively initiate the metal deposition process.

In our experiment, we first washed commercial Kevlar fibers with acetone and IPA to remove a majority of dust and organic residues from the manufacturing process. Then, a nitration/reduction treatment is applied on the washed fibers, which is illustrated in Figure 5.2.
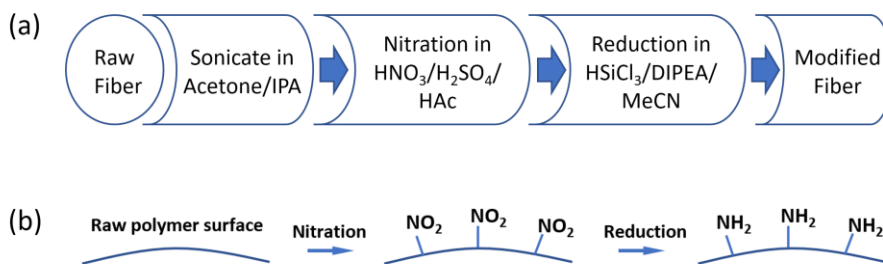
Figure 5.2. (a) Flow chart of the cleaning and nitration/reduction surface treatment process; (b) Illustration of the surface chemistry during nitration/reduction, which results in a Kevlar surface terminated by amine groups.

The nitration process was performed using a 1:1:1 concentrated nitric acid (HNO_3), sulfuric acid (H_2SO_4) and acetic acid (HAc) mixed acid bath at room temperature for 5 hours. The nitrated Kevlar fibers are then thoroughly rinsed with DI water, and dried in oven at 140 °C for 2 hours to remove absorbed acid and water. Afterwards, the fibers are transferred directly into a reducing bath, which was a recipe modified from a previously reported method.[123] Briefly, nitrated fibers mounted onto a glass holder are submerged into 0.5 mol/L N,N-diisopropylethylamine (DIPEA) solution in 50 mL MeCN (anhydrous), which was ice cooled to 0 °C beforehand. The mixture is sealed in a glass bottle with a rubber cap. Then, 1.8 mL of trichlorosilane ($HSiCl_3$) is added to the mixture dropwise over 1 hour through a hypodermic needle. The reduced fibers are finally taken out of the bath and rinsed with MeCN, water and IPA, consecutively.
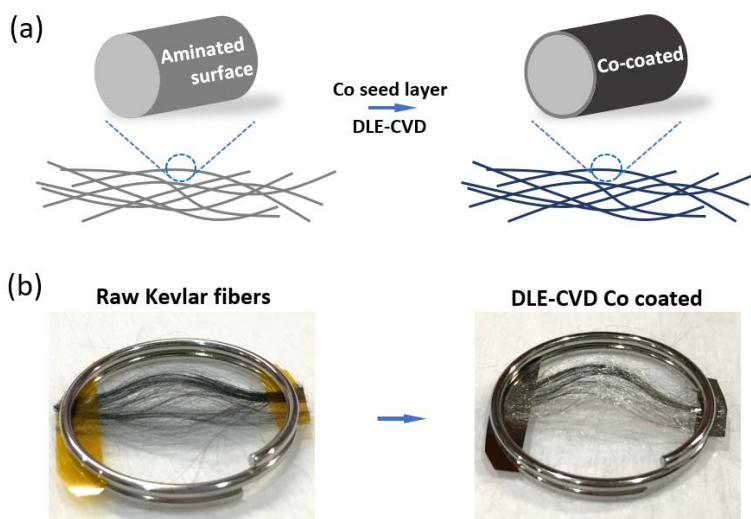
Figure 5.3. (a) Scheme of the DLE-CVD Co surface metallization of aminated Kevlar fibers; (b) Photo of the raw Kevlar fibers and the Co-coated Kevlar fibers mounted on a key ring clip; Soft Kapton sheets were used as gaskets between the fibers and metal clip.

After cleaning and nitration/reduction surface modification, we then coated the fibers with Co DLE-CVD. Figure 5.3 shows the scheme and actual photos of raw fibers and Co-coated fibers mounted on a ring clip sample holder. For firm fixture of Kevlar fibers onto the holder, Kapton sheets were inserted between the fibers and metal clip as gaskets. After 15 min deposition (~25 nm Co coating), all Kevlar fibers are visibly coated and exhibit a metallic silver color.
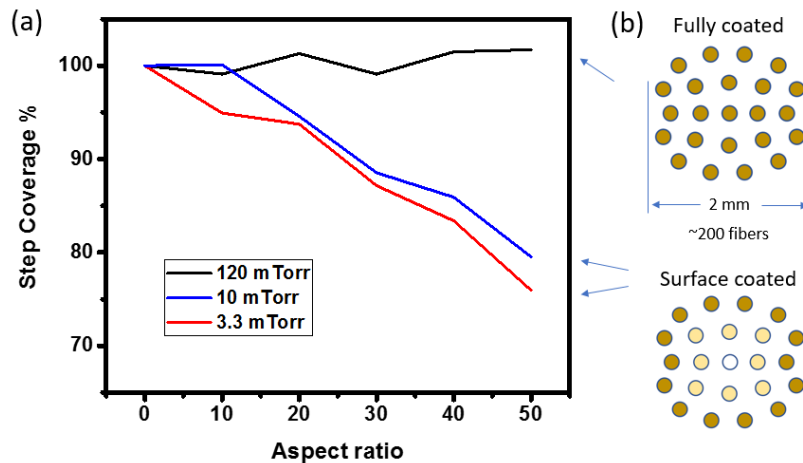
Figure 5.4. Step coverage percentage at various depth of a trench (thus various aspect ratio) of the thin films deposited with 120 mTorr, 10 mTorr and 3.3 mTorr precursor partial pressures.

In the Co DLE-CVD process, precursor partial pressure was steadily regulated to be at 120 mTorr, which is 1 order of magnitude higher than the precursor vapor pressure offered by traditional CVD with the same Co precursor. The reason to use such a high precursor vapor pressure is to achieve saturated thin film growth on all fibers inside a

bundle. Figure 5.4(a) shows that with a precursor partial pressure at 120 mTorr, near

100 % step coverage is achieved in a complex structure with aspect ratio up to 50:1.

However, when a precursor partial pressure of 10 mTorr or lower is used, less than 80 %

of step coverage are observed at 50:1 aspect ratio. When it comes to fiber bundle

metallization, full coverage of all fibers was only achieved with 120 mTorr precursor

vapor pressure, while lower vapor pressures resulted in surface-coated fiber bundles, as

illustrated in Figure 5.4(b).
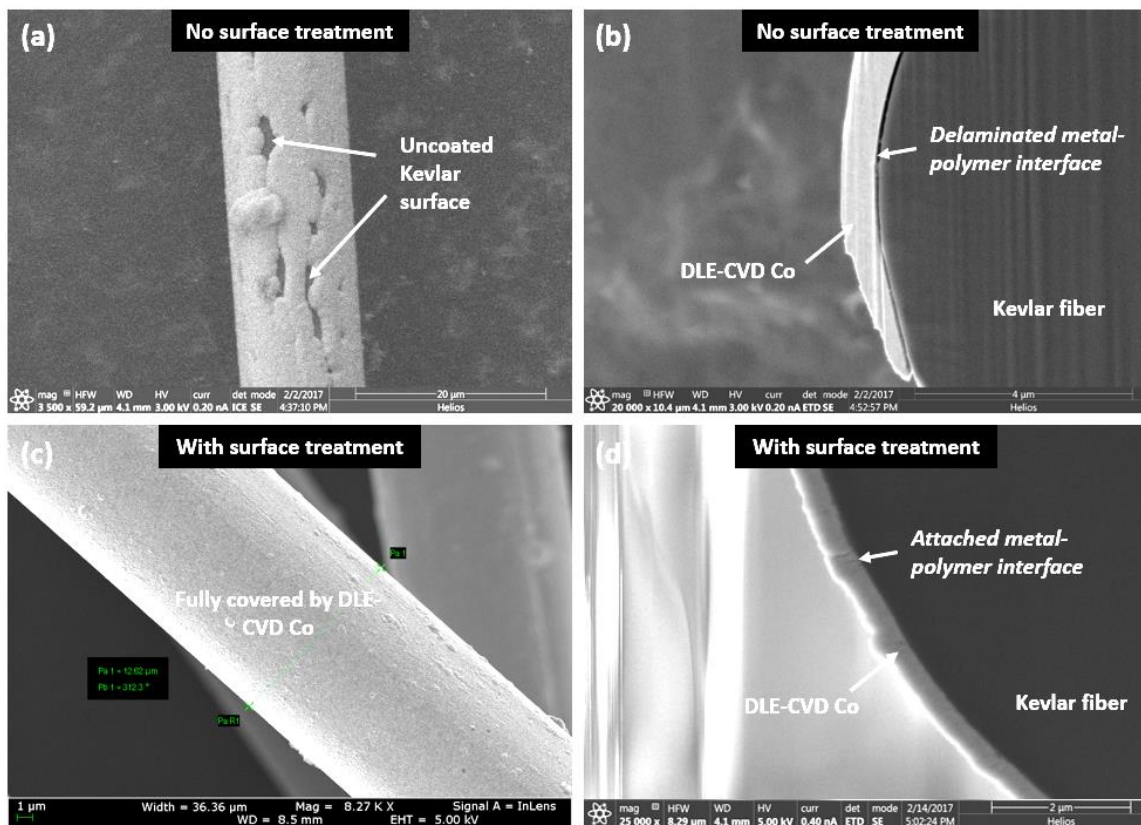
Figure 5.5. (a) Uncoated/exposed surface of a Co-coated Kevlar fiber without surface

pre-treatment; (b) FIB cross-section image of a Co-coated Kevlar fiber without surface

pre-treatment, showing delaminated metal-polymer interface; (c-d) Co-coated Kevlar fiber with proper surface cleaning and modification before deposition.

SEM images of the Co-coated Kevlar fibers with and without surface treatment are shown in Figure 5.5. Exposed Kevlar surface (insufficient nucleation sites) and delaminated metal-polymer interface (poor adhesion) were observed on the coated Kevlar fibers without the above-mentioned nitration/reduction surface treatments. These phenomena in the metallization layer are highly unfavorable for flexible electronics, since they will severely decrease the conductivity and reliability of metallized fiber interconnects. In contrast, after surface cleaning and modification, fully covered Kevlar surface and well-attached metal-Kevlar interface were achieved, as shown in Figure 5.5 (c-d). These results indicate that proper surface treatments of polymer fibers before metal deposition processes are highly critical in order to obtain high-quality metallization layers on the fibers.

5.5   Electroplating on DLE-CVD Co Seeded Kevlar Fibers

DLE-CVD Co provide highly conformal, uniform and continuous metallization layer on Kevlar fiber bundles. Whereas, some applications require different kinds of metal coating on the metallized fiber surfaces. For example, copper is preferred as high-current interconnect conductor material because of its high bulk conductivity. In this regard, DLE-CVD Co can serve as a seed layer for electroplating desired metal coatings,

including copper, onto Co-coated fibers. Herein, we use copper electroplating as an example to demonstrate that core-shell Kevlar fibers with multiple surface metallization layers can be achieved onto our DLE-CVD Co seed layer.

The electroplating process was conducted with a home-built electrochemical apparatus. Electroplating solution was modified from a previously reported alkaline bath.[124] Of note, strongly acidic bath was avoided for our metal electroplating experiments because Co can be slowly etched by acids with the absence of a bias. To make our plating bath, 0.1 mol/L $CuSO_4 5H_2O$, 0.1 mol/L $(NH_4)_2SO_4$ and 0.8 mL/L concentrated ammonia solution are first dissolved in DI water. Then roughly 15 mL/L ethylenediamine is slowly added to the solution with mild stirring in a fume hood, until a clear purple solution is formed. The pH of the final plating bath is 9~10, which is slightly basic. The electroplating process was done with a constant 2 mA/cm^2 current density, and 0.7~1.0 V potential on the working electrode. A polished pure copper rod was used as the anode and nickel clips were used to mount the samples.

To study the basic electroplating characteristics, we first performed experiment on planar glass and silicon substrates. As shown in Figure 5.6, DLE-CVD Co creates highly smooth and reflective surface, and electroplated Cu attached firmly onto our DLE-CVD Co seed layer, forming a mirror-like copper finish. The AFM rms of these two surfaces are measured to be 1.0 nm for Co and 5.0 nm for Cu. The electroplating process lasted 6 min and formed ~120 nm Cu coating, which gives a deposition rate of 20 nm/min.
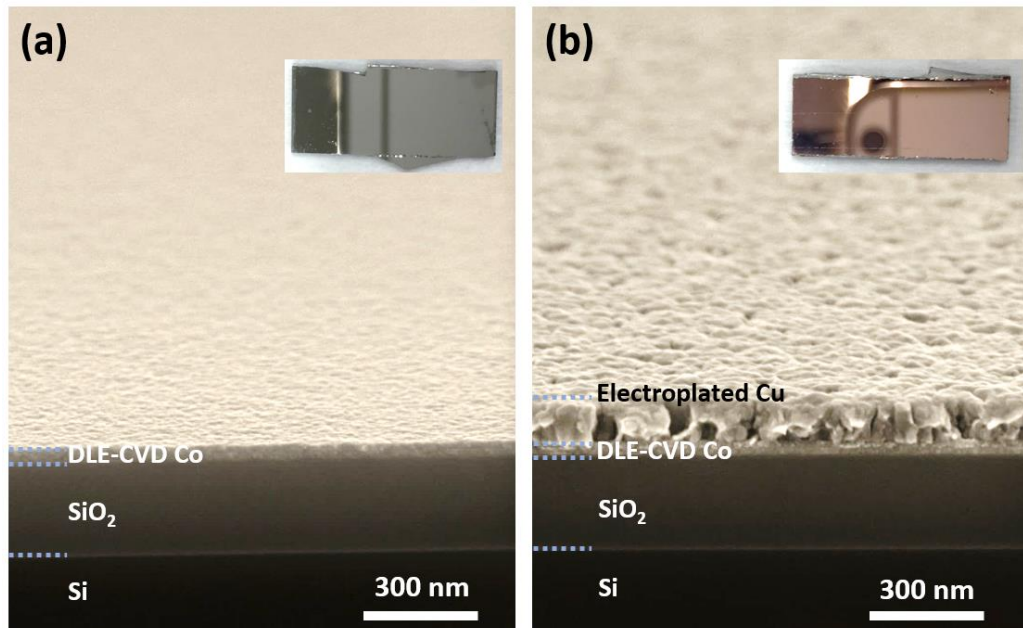
Figure 5.6. (a) Cross-section SEM image of 40 nm DLE-CVD Co deposited on a silicon substrate with thermal oxide; (b) Cross-section SEM image of 120 nm Cu electroplated onto 40 nm DLE-CVD Co seed layer. The insets of the figures are optical images showing the smooth mirror-like surface of DLE-CVD Co and electroplated Cu on glass substrates.

The same deposition processes are then applied to Kevlar fibers. The fibers are first cleaned, surface treated, dried, and mounted on a nickel key ring clip with Kapton gaskets as described in previous context. 25 nm DLE-CVD Co are deposited onto the fibers as seed layer. The key ring clip (1-inch diameter) with the Co-coated fibers are then directly connected to the cathode and submerged into our basic plating bath, followed by 10 min Cu electroplating (~200 nm Cu) with 8 mA current and 0.7 V bias. Figure 5.7 shows the optical images of Kevlar fibers before and after electroplating. All

fibers visibly turned from the metallic silver color of Co to a bright copper color,

indicating that all fibers are uniformly coated with both DLE-CVD Co and electroplated

Cu, because any discontinuity in the Co seed layer will result in uncoated areas after Cu

electroplating.
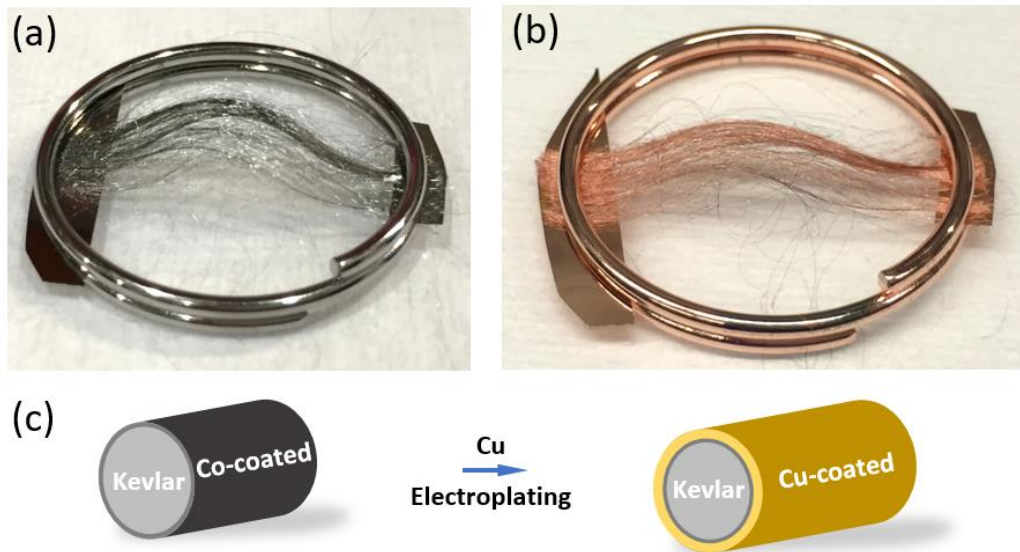
Figure 5.7. (a) DLE-CVD Co coated Kevlar fibers; (b) Cu coated Kevlar fibers after

electroplating onto Co seed layer; (c) Schematic illustration of the formation of

Kevlar/Co/Cu core-shell fiber structure.

SEM images of the Co/Cu-coated fibers are shown in Figure 5.8. All fibers are

uniformly coated; no delamination or uncoated area was observed over large areas. The

surfaces of the coated fibers are highly smooth, which is similar to the results obtained

on planar test samples. The high Cu coverage of Kevlar fibers after electroplating should

be attributed to the high conformality of our DLE-CVD Co process, which metallized all

fiber surfaces even for the inside parts of the fiber bundle, providing conduction

pathways for electroplating.
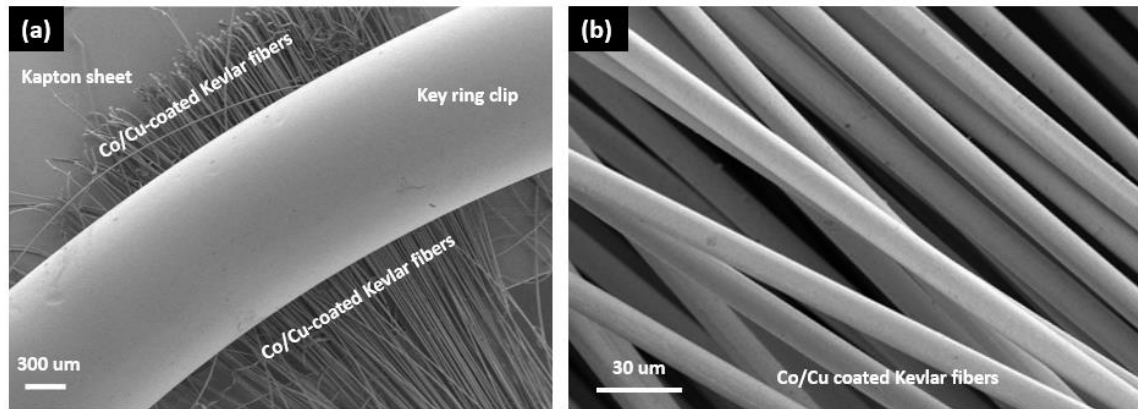
Figure 5.8. (a) Low-mag SEM image of Co/Cu-coated Kevlar fibers clamped between

Kapton gasket and metal clip; (b) High-mag SEM image of Co/Cu-coated Kevlar fibers,

showing highly uniform and smooth surface metal coverage.

To characterize the Co/Cu-coated fibers better, we performed FIB cross-section

imaging of a coated fiber. Figure 5.9(a) presents the overall cross section of the fiber

(~11 um diameter), demonstrating all-around metal coverage on the surface. Figure

5.9(b) is a magnified SEM image at the interface with enhanced brightness and contrast,

which clearly shows both layers of Co and Cu, as well as the well-attached

metal/polymer and metal/metal interfaces. The magnified image in Figure 5.9(c) shows

attached polymer/metal interface over a larger area around the bottom edge. These

results prove that our metallization processes can create multi-layer high-quality metal

coatings on fiber bundles. In future work, we can potentially fabricate multiple shells

that are electrically separated by insulating layers, e.g. ALD Al_2O_3 or SiO_2, creating micro-/nano-scale co-axial fibers for next-generation flexible electronic devices.
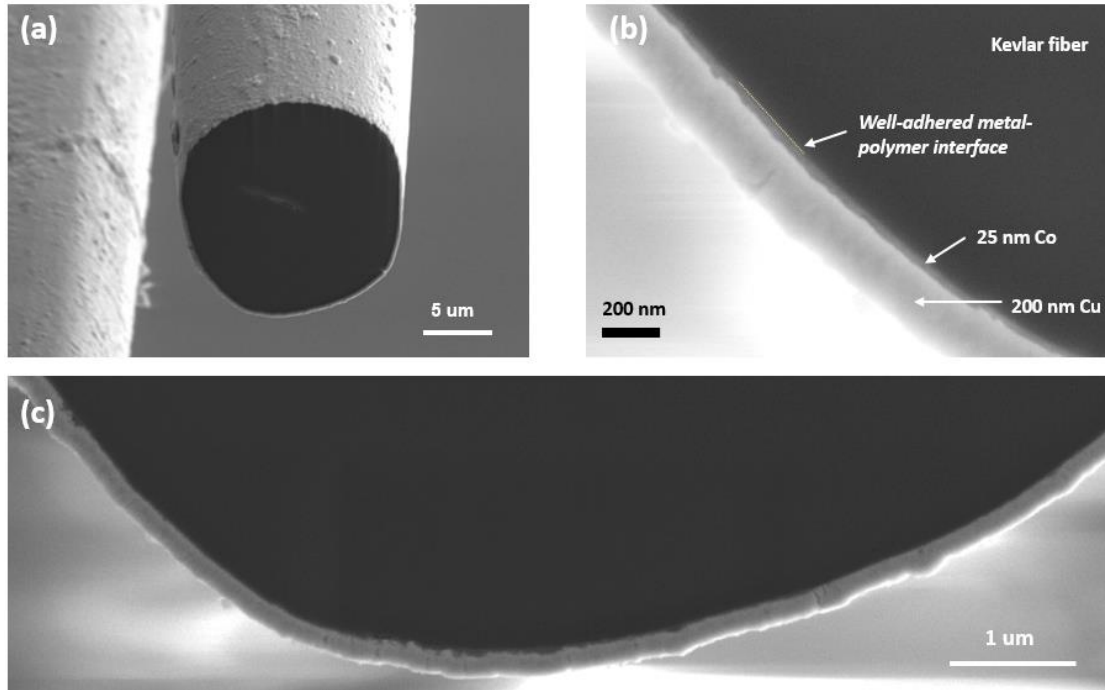
Figure 5.9. (a) FIB cross-section image of a Co/Cu-coated Kevlar fiber; (b) Magnified image of the same fiber, clearly showing each layer of the metal shells; (c) Magnified image around the bottom edge, showing fully attached polymer/metal interface.

So far, we have successfully demonstrated metallization processes of Kevlar fibers with 10~12 um diameters. To test the potential of our DLE-CVD processes in applications where smaller nano-scale flexible interconnects are needed, we used electrospun Nomex fibers with <1 um diameters as an example. After depositing 25 nm DLE-CVD Co and ~120 nm electroplated Cu onto the electrospun fibers, FIB cross-section imaging

was performed. As shown in Figure 5.10(a), two Nomex fibers with 1 um and 0.6 um diameters are coated with DLE-CVD Co. The cross-section presents conformal all-around coating for both fibers, despite that the contacted part between the two fibers is coated with less film. However, this issue may be resolved by introducing mechanical vibrations to the fibers during deposition. Figure 5.10(b) shows clear and attached Co/polymer interface, indicating that our DLE-CVD process is also effective to create high-quality surface nucleation and adhesion on high-curvature surfaces (small-diameter fibers).
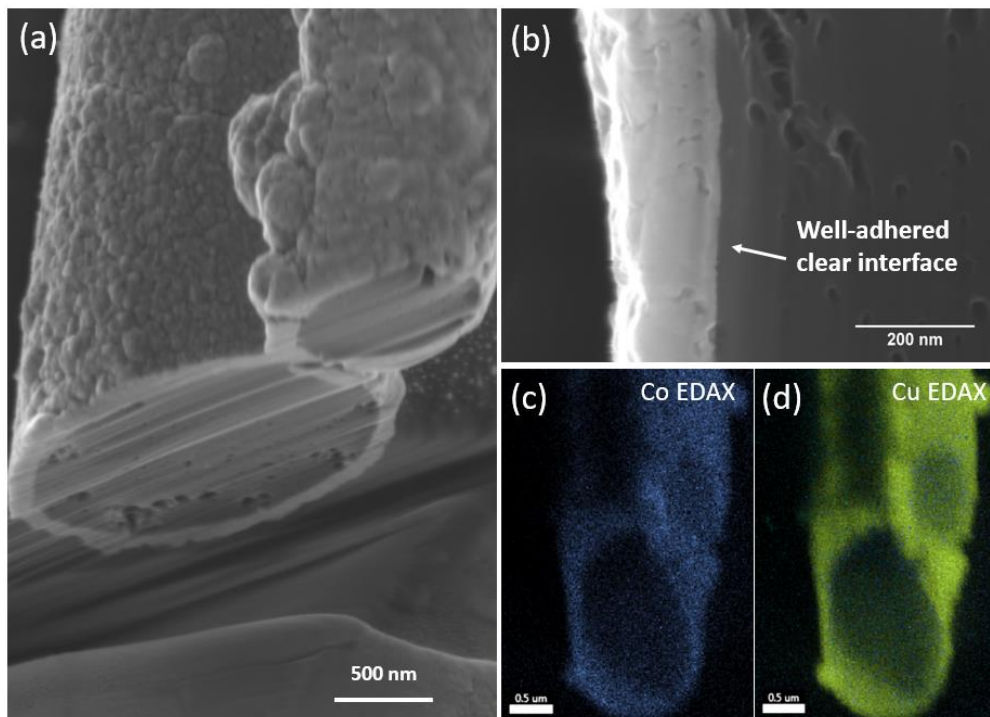
Figure 5.10. (a) Nano-scale Nomex fibers coated with DLE-CVD Co and electroplated Cu; (b) Well-adhered metal/polymer interface; (c-d) EDAX mappings of the coated fibers.

Figure 5.10(c and d) present the cross-section EDAX elemental mappings of Co and

Cu on coated fibers. Both metals were observed on the fiber surface, proving that the

coated materials are indeed Co and Cu metals. Successful electroplating of Cu onto the

Co-coated Nomex fibers reveals that the DLE-CVD Co is highly continuous and

conductive, which is an important metric of high-quality seed layers. The Cu layer

formed on top of DLE-CVD Co show strong metal-to-metal adhesion, no delamination

was observed, which suggests the DLE-CVD Co surface is clean, conductive, and

accommodates sufficient nucleation sites for electroplating. These experiments provide

evidence that our DLE-CVD Co is a promising technique to create high-quality initial

metallization layers for nano-scale fibers, which should be attributed to its high

controllability, conformality and uniformity.

5.6   Demonstration of Conductivity and Flexibility of Metallized Kevlar Fibers

In this section, we use two simple test setups to demonstrate the potential of our

metallized Kevlar fibers as interconnects of flexible electronics. All fibers used in these

tests are Kevlar fibers coated with 25 nm DLE-CVD Co and 125 nm electroplated Cu.
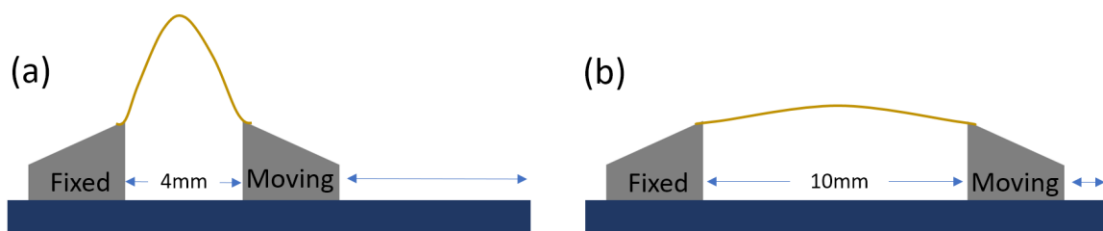
Figure 5.11. Single fiber bending test. (a) Bended state; (b) Extended state.

In the first setup, we attach a 10-mm long coated fiber to two metal arms by silver paste, as shown in Figure 5.11. One of the arms is fixed to the substrate, and the other one is a moving arm controlled by an actuator mechanism. The moving arm then starts to repeatedly move from 10 mm position (fully straightened fiber) to 4 mm position (bended fiber), at a frequency of 1 bend per second. Conductive wires are connected to both arms and measures resistance as the bending proceeds. The initial resistance of the wire was 2.3 ohm, and after 10000 bending cycles, the resistance remained the same. This test indicates that the coated fiber can sustain bending with less than 2 mm radius of curvature. The bending test herein is a proof that our coated fiber is flexible and conductive, and the resistance does not change as the bending process proceeds, fulfilling the basic requirements for flexible interconnects.
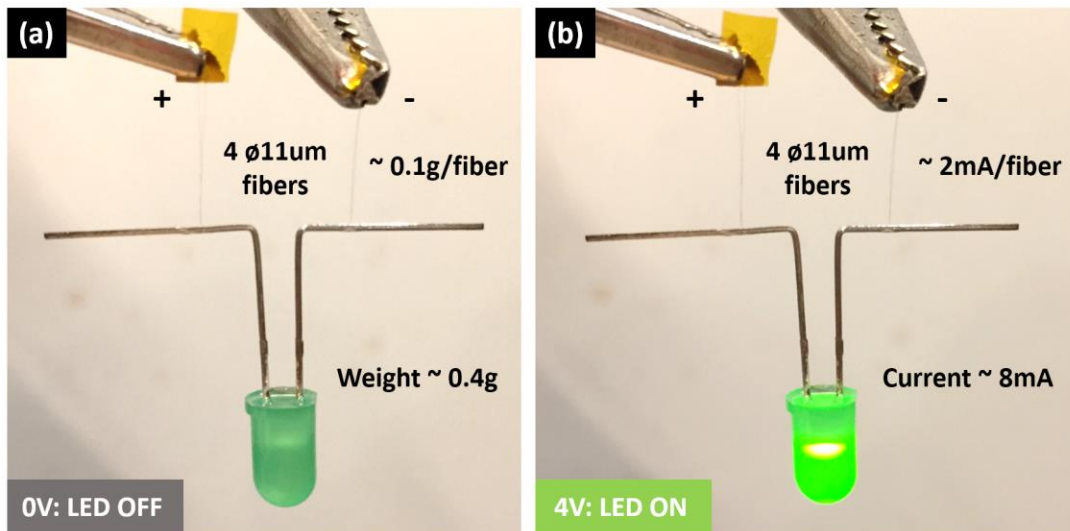
Figure 5.12. (a) A 0.4 g green LED suspended by 4 single coated fibers; (b) 8 mA current applied through the fibers to light up the LED.

In another test, we use 4 single Co/Cu-coated Kevlar fibers with 11 um diameters to suspend and power a 0.4 g green LED. As shown in Figure 5.12, the fibers are glued onto two Kapton sheets with conductive silver paste, which are then connected to a sourcemeter by alligator clips. After attaching the LED onto the wires, each single wire suspends 0.1 g of weight, which is equivalent to $1.0 \times 10^7 \, N/m^2$ (10 MPa). With 8 mA of current powering the LED, the current density on each fiber is 84 $\mu A/\mu m^2$.

5.7   Conclusions

In this chapter, we present the potential application of DLE-CVD process in the surface metallization of polyaramid fibers. Complete all-around coating for all fibers even in the form of bundles were achieved with our process, due to the ultrahigh step coverage offered by DLE-CVD. Surface nucleation and interfacial adhesion issues were resolved by introducing amine groups onto the surface with a nitration-reduction chemical treatment before metallization. With our highly uniform and conformal DLE-CVD Co as the starting seed layer, specific kinds of metal (e.g. Cu) can be readily electroplated onto the Co layer, enabling the fabrication of multi-layer flexible conductive interconnects. Furthermore, flexibility and conductivity of the Co/Cu-coated Kevlar fibers are demonstrated with two simple test setups. These results provide prototype demonstrations of potential future application of surface-metallized fibers in flexible electronic devices, and DLE-CVD offers the feasibility of producing high-quality metallization on the surface of polymer fibers.

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