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Abstract
In this paper we describe the technological and fabrication methods necessary to incorporate both photonic and electronic-band engineering in order to create novel surface-emitting quantum cascade microcavity laser sources. This technology offers the promise of several innovative applications such as the miniaturization of QC lasers, and multi-wavelength two-dimensional laser arrays for spectroscopy, gas-sensing and imaging. This approach is not limited to light-emitting devices, and may be efficiently applied to the development of mid- and far-infrared normal-incidence detectors.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The recent demonstration of laser action in a photonic-crystal quantum cascade (PC QC) laser [1] proved that photonic- and electronic-band engineering can be successfully combined to add new functionalities to devices based on intersubband transitions [2–4]. The core idea is the use of a high-index contrast planar two-dimensional (2D) photonic crystal that can act as the resonator providing feedback necessary for lasing, and at the same time can diffract light vertically up from the surface of the semiconductor chip. In particular the size reduction, compared to standard QC technology, opens the way to the miniaturization and on-chip integration of intersubband devices for a broad range of applications. Novel processing recipes and procedures were necessarily developed to demonstrate the first functional PC QC microcavity laser. The purpose of this paper is to report the fabrication technology to the scientific community.

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QC lasers are intrinsically in-plane emitters because of the transverse magnetic (TM) polarization of intersubband (ISB) transitions. The same principles of physics imply that detectors based on ISB transitions are inefficient if used in a normal-incidence configuration (i.e. when the light incident on the device travels in a direction transverse to the epitaxial layers). For instance, quantum well infrared photo-detectors (QWIPs) intrinsically require in-plane light [5] and would benefit from a technique to make them surface-radiation accessible. The very same technology we developed for ISB emitters should also be applicable to develop efficient normal-incidence intersubband detectors with built-in resonators.

2. Strategy, design and pattern writing

The design of the PC QC microcavity, described in more detail elsewhere [1], is briefly summarized here. The PC used consists of a hexagonal etched array of air holes, chosen not for the frequency band-gaps it forms (in 2D this lattice does not have a complete in-plane band-gap for TM-polarized light), but rather because of its connected nature, necessary for straightforward electrical injection. The main criterion is that the photonic lattice provides high-index contrast so

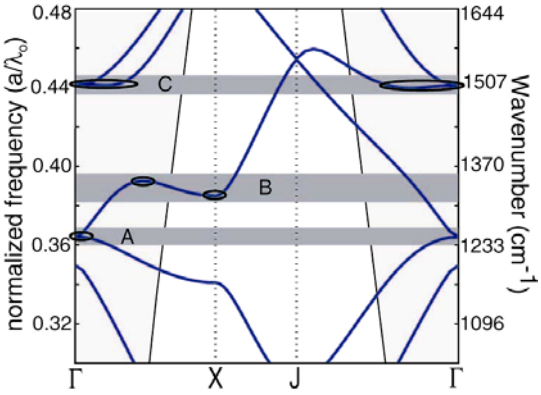

Figure 1. Calculated two-dimensional in-plane transverse-magnetic band-structure for a hexagonal lattice of air holes ($r/a = 0.30$, $n_{\text{eff}} = 3.345$). The flat-band regions, labelled A, B and C, are indicated by dark grey bands.

that strong optical feedback can be obtained over several lattice periods, setting the scale of the PC laser devices. We calculated the in-plane band-structure for TM-polarized light (figure 1) using the plane wave expansion method [6]. In the regions with flat dispersion, low-loss resonant modes can be localized in *finite* lattice structures (such as the cavities described below) due to the reduction in group velocity over an extended region of wavevector space [1]. Especially important to this work are the three frequency regions highlighted in dark grey in figure 1, as they surround the flat-band regions in the frequency range close to the second-order Bragg condition. To overlap these band-edge resonances with the QC material gain spectrum ($\lambda \approx 8\ \mu$m), two-dimensional arrays of devices were fabricated using the procedure described below. The values of the lattice spacing (a) and the hole radius (r) were systematically varied from device-to-device, allowing for the PC modes to be tuned through the QC gain peak.

A general layout of the processing steps is reported in figure 2: it shows a pictorial view of a cleaved device during the different phases of the processing.

After a hard mask layer of silicon dioxide (SiO_2) 500 nm thick was deposited by plasma-enhanced chemical vapour-deposition (PECVD), the PC pattern was written using electron beam lithography on a JEOL 9300FS 100 kV system (figure 2(a)). We used a commercially available environmentally stabilized chemically amplified photo-resist (ESCAP), UV113, which was developed as a 248 nm DUV resist (figure 3). The chemically amplified resist was chosen because it features a good resolution and etching resistance, and it also requires a significantly lower dose than conventional single component resists. This allowed us to better populate our samples with practical writing times, an important requirement in view of the realization of 2D arrays of PC QC lasers with hundreds of micro-devices on a single semiconductor chip. The patterned e-beam resist was transferred to the underlying silicon oxide hard mask layer via reactive ion etching using CHF_3, typically a 20–40 min etch. The remaining resist was then solvent removed (figures 2(b) and 4(a)).

The choice of SiO_2 as a hard mask instead of Si_xN_y was dictated by the much steeper sidewall angle achievable with silicon dioxide. Figure 4(a) shows that almost vertical

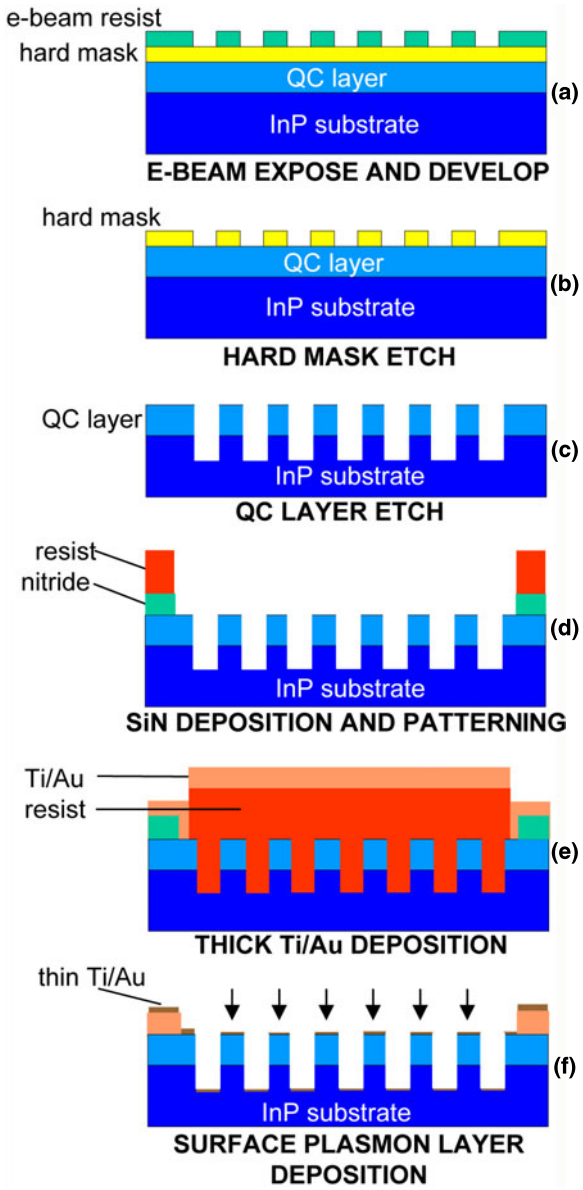

Figure 2. Pictorial layout of the processing steps necessary to fabricate a PC QC device: (a) SiO_2 hard-mask deposition and e-beam resist patterning. (b) Transfer of the e-beam pattern to the underlying SiO_2 layer and resist removal. (c) Semiconductor etch via ICP-RIE and removal of the SiO_2 mask. (d) SiN deposition and its removal, via optical lithography and RIE etch, at the PC device sites. (e) Deposition of the thick (30/300 nm, Ti/Au), low resistance contact up to the border of the devices, using contact optical lithography. (f) Last step: *vertical* evaporation of the thin (10/100, Ti/Au), surface-plasmon carrying layer. This layer must also provide the topside electrical contact, while avoiding shorting of the same contact to the substrate.

sidewalls were obtained with silicon dioxide. On the other hand, silicon nitride (figures 4(b), (c)) exhibited angled sidewalls that would negatively affect not only the r/a ratio of the PC, but the quality of the semiconductor etch too.

It proved critical to clean the polymeric build-up which occurs during the hard mask etching step (figures 5(a), (b)) in order to obtain a high quality transfer of the PC pattern into the active semiconductor layers. This was accomplished via a combination of oxygen plasma followed by a vigorous

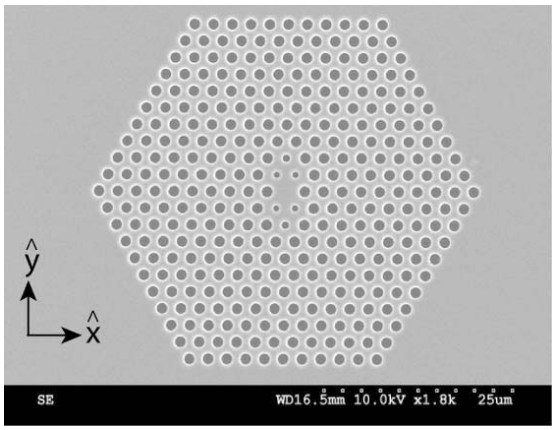

Figure 3. SEM image of a typical device after e-beam writing.

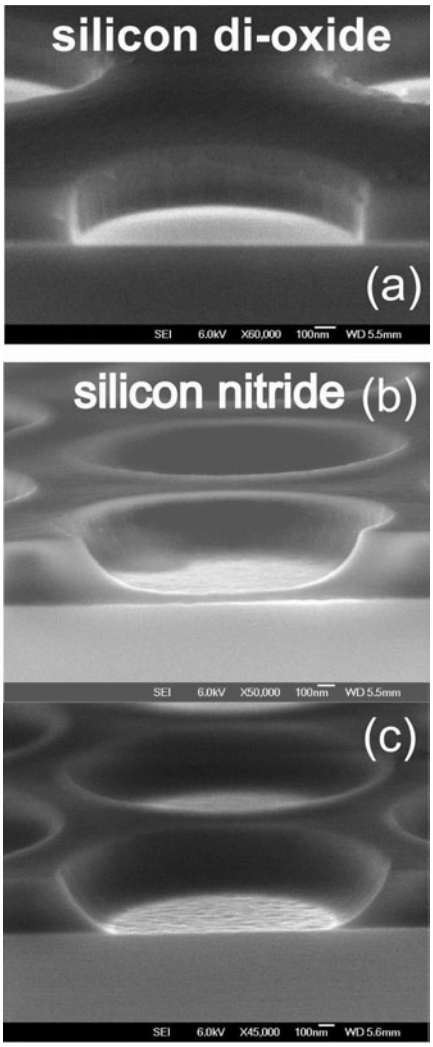

Figure 4. SEM image of a cleaved device after the mask transfer, but before the semiconductor etch: (a) SiO_2 mask, exhibiting a perfectly vertical profile. The thickness of the silicon dioxide mask is 500 nm. (b), (c) Si_xN_y masks, exhibiting angled sidewalls. The lack of verticality is not due to excessive etch time, since the sidewalls are tilted even before the complete removal of the mask (panel (b)).

spray of acetone with a high pressure gun. Figure 5(a) shows that a thin layer of polymer tends to cover the whole sample, but its accumulation is particularly massive at the periphery of the holes in the insulator (figure 5(b)). This latter effect is probably due to a combination of chemical and kinetic phenomena. Figures 5(c), (d) show the patterned hard mask after the removal of the build-up: the clean-up procedure was successful.

3. Semiconductor etching

The transfer of the PC pattern to the semiconductor material (figures 2(c) and 6) was achieved using an Oxford Instruments Plasma Technology inductively coupled plasma reactive ion etch (ICP/RIE). The three primary requirements on the etch were:

(1) the etched holes need to extend through the core region significantly (∼2–3 μm) into the lower cladding, in order to minimize substrate radiation losses,
(2) the etched holes need to be vertical to reduce loss and avoid an electrical short between the top contact and the substrate, as described in the next section, and
(3) the etched sidewalls should be as smooth as possible to reduce losses (in addition to scattering loss, significant erosion of the core layer can reduce its effective index and potentially increase vertical radiation losses).

Dry etching of In-containing III–V semiconductor materials is typically accomplished using one of two gas chemistries [7]. The first, using a CH_4/H_2 mixture, is performed at room temperature but is relatively slow ($<$60 nm min^{-1}) and suffers from heavy polymer deposition during the process. Cl_2-based plasmas have also been used, but the low volatility of $InCl_x$ products at room temperature requires some form of heating to be employed. One method for producing smoothly etched, vertical sidewalls in an InP-based semiconductor system is direct heating of the wafer table ($>$150 °C). Such a process has been employed [8] to produce sub-micrometre width racetrack resonators with a measured quality factor (Q) of 8000. More recently [9], a similar high temperature ($T = 205$ °C) etch was used to create high-Q ($Q \sim 13\,000$) near-IR PC microcavities InP-based multi-quantum well material.

The Cl_2-based plasma etch that we employ here does not make use of direct wafer table heating, but rather uses the high-density plasma produced by the ICP system to provide local surface heating of the sample and an increased efficiency in the sputter desorption of the $InCl_x$ products [7]. Such an etch has been used by Fujiwara *et al* [10] to etch 8 μm diameter, 3.6 μm deep holes in a photonic band-gap structure.

The ICP-RIE etch was studied as a function of ICP power (300–500 W) and RF power (100–350 W), with the chamber pressure ($P_{ch} = 3$ mTorr) and Ar:Cl_2 gas chemistry (12 sccm:8 sccm) kept fixed, and no He backside cooling. The final ICP and RF powers chosen were 350 and 250 W, respectively, and produced vertical sidewalls with an acceptable amount of sidewall roughness (figure 6). Lower RF powers produced extremely pitted (and slightly angled) sidewalls throughout both the core and cladding layers (which we attribute to the decreased volatility of the $InCl_x$ etch products, resulting from the lower sample temperature and/or lower desorption rate caused by the reduced RF power),

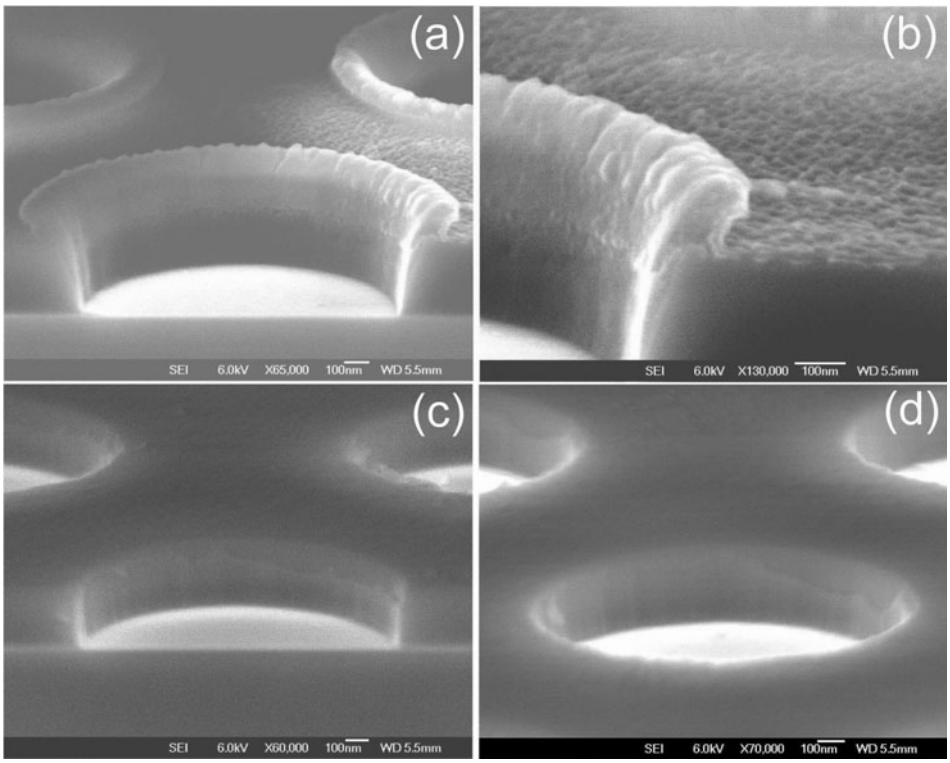

Figure 5. (a), (b) SEM images of a representative device immediately after etching the SiO_2 mask with CHF_3 plasma RIE. The polymeric build-up occurs during the hard mask etching and it is mostly localized at the edges of the holes (panel (b)). (c), (d) SEM images of typical devices after cleaning with a combination of oxygen plasma followed by a vigorous rinse of acetone with a high pressure spray.

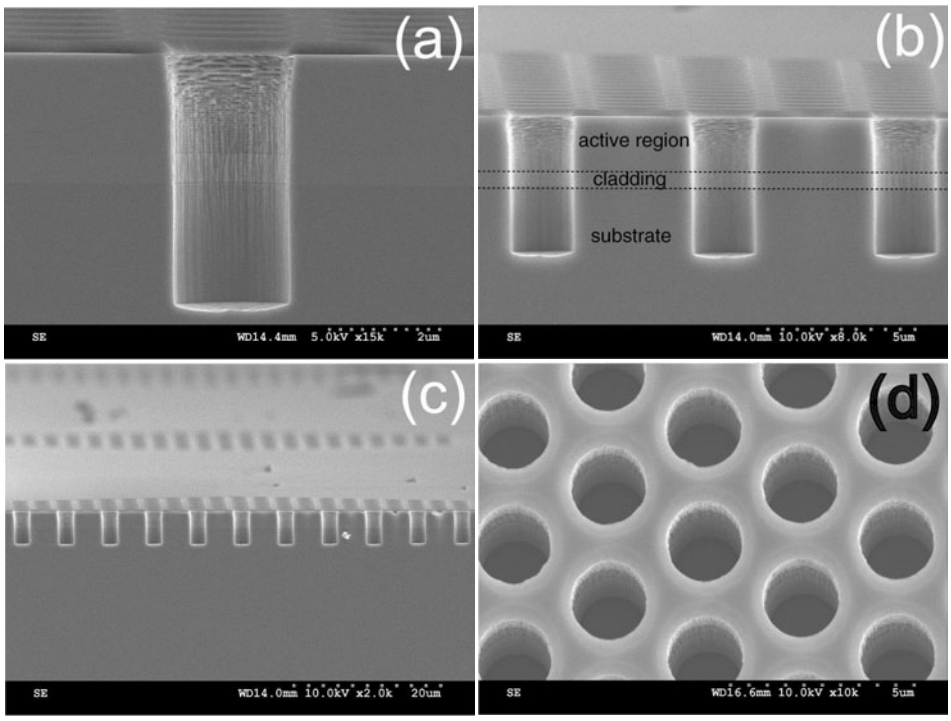

Figure 6. SEM images of a typical device after the semiconductor etch, but before the deposition of electrical contacts. (a)–(c) Images of a cleaved devices at different magnifications, showing the high quality, smoothness and verticality of the etch (panel (a)); the etch-depth compared to the active region thickness of the QC device (panel (b)); and the remarkable uniformity of the etch across the whole device (panel (c)). (d) SEM image of a device from the top surface.

while higher RF powers created smooth sidewalls in the lower cladding and InP layers but increased roughness in the core layer (attributed to pitting that occurs in Al-containing layers that are etched at too hot a temperature). Similar effects on the

sidewall roughness were observed as the ICP power was varied. These results suggest that the sample temperature (generated by the plasma) is a leading factor affecting sidewall roughness. The percentage of Cl_2 in the gas mixture, which can also play a role, has been varied between 30 and 50%, with a value of 35% (7 sccm) finally chosen as the best compromise between decreased sidewall roughness (seen for lower Cl_2 percentages) and improved sidewall angle (seen for higher Cl_2 percentages). For our typical etch times ($t \sim 4.75$ min), etch depths of 5 μm are achieved.

Using the plasma as a mean of increasing the sample temperature indicates that the etch rate (and therefore etch depth) will be a nonlinear function of time, as some amount of time is required for the temperature to equilibrate at a value hot enough for the $InCl_x$ compounds to be sufficiently volatile. This has been observed experimentally as etch times under 3 min have produced devices with angled holes and non-volatile $InCl_x$ etch products. Note that the change in sample temperature as a function of time for a number of different process parameters has been investigated in detail by Thomas III, *et al* [11], and confirms that some minimum etch time (dependent upon the RF and ICP powers) is required for the sample to reach the requisite temperature ($>150\,^{\circ}$C).

Our etch creates a nearly 90° sidewall angle but suffers from roughness in the core layer. We believe that this is the result of the elevated sample temperature created by the high density plasma, which probably causes pitting of Al-containing layers.

In the optimal case, control of the sample temperature (or some other critical process parameter) as a function of time would be employed to allow for varying etch conditions depending on the layer composition. This will be of particular use in standard vertical waveguide designs which have both top and bottom semiconductor cladding layers (often composed of AlInAs).

4. Application of electrical contacts

The next and final step of the device fabrication consists in the application of electrical contacts, necessary to pump energy (i.e. current) through the system (figures 1(d)–(f)). It is important to emphasize that unipolar devices are not affected by leakage currents due to surface recombination, which are usually substantially increased (for interband lasers) by the etching of the PC pattern into the semiconductor material. The ease of electrical pumping in fact makes this an ideal model system for fundamental studies of photonic crystals in linear, non-linear and near-field optics [12].

The essential requirements we need to satisfy in order to fabricate a functional device are the localization of current injection into the PC QC devices, and the absence of metal deposition onto the holes' sidewalls (to reduce losses and avoid device shorting from the top contact to the substrate). In addition, no mesa will be etched around the devices so as to rule out other feedback mechanisms for the laser and confirm that the PC itself is acting as a microcavity.

An insulating layer of silicon nitride (300 nm thick) was deposited on the sample. Hexagonal windows were opened in the insulator at the PC device sites via reactive ion etching using CF_4. Contact optical lithography has been used with an image reversal process using AZ5214-IR photo-resist from Clariant. The use of image reversal photo-resist was found to improve the yield, as the severe topography creates difficulties for conventional positive resist processes. In the absence of a mesa, only the openings in the insulator silicon nitride pattern therefore define the regions of current injection.

A thick, low resistance Ti/Au (30/300 nm) contact was patterned up to the border of the hexagonal device areas using liftoff from a single layer positive resist (Shipley 1813), followed by the cleaning procedure (figures 1(e), (f) and 7(a), (b)). After the sample was thinned to $\approx$300 μm with an alumina polish from the back side, a metal back-contact comprised of Au/Ge/Ag/Au (12/27/50/300 nm) was e-beam evaporated. As a last step, a vertical evaporation and lift-off of thin Ti/Au (10/100 nm) was performed again using the image reversal photo-resist described above (figures 7(a)–(c)).

The final deposition of a thin Ti/Au contact plays an essential role in these devices. Although pure gold is a better surface-plasmon carrying material at these wavelengths [13, 14], we introduced a very thin layer of Ti for sticking purposes. Tests performed on surface-plasmon QC lasers processed as regular stripes showed no increase in the threshold current density when the thin layer of Ti was introduced. The stringent requirement for vertical sidewalls in the active semiconductor etch is now evident, since this latter metal deposition must provide the topside electrical contact while preventing shorting of the same contact to the substrate. Metal is thus deposited between the holes and on the bottom of the holes. Only a limited amount of Ti/Au is deposited on the sidewalls, as shown in figure 7(d).

5. Device characterization

The final devices (figure 7(c)) were soldered with indium to a copper block, wire bonded, and mounted in a He-flow cryostat for the optical and electrical measurements at a temperature of 10 K.

The current–voltage (I–V) characteristic of a typical device at 10 K (figure 8(a), dashed curve) proves that the device fabrication was successful and the large sidewall surface of the holes and the deposited metal does not contribute to the leakage current. On the other hand, the somewhat soft turn-on of the I–V is most certainly due to poor current confinement, since no mesa was fabricated around the devices. Etching a mesa around the PC would avoid current dispersion and increase current confinement. However for the first demonstration the absence of a mesa has been a key feature since it rules out other feedback mechanisms (Fabry–Perot and whispering gallery like reflections) and confirms that the PC itself is acting as a microcavity [1].

The light–current (L–I) characteristic of the same device at 10 K is reported in figure 8(a) (solid curve). The maximum power emitted from the semiconductor surface is in the range 400 μW to 1 mW, depending on the device. The L–I characteristic in log-linear scale is shown in figure 8(b). The transition from spontaneous to stimulated emission and a sharp laser threshold are clearly identifiable. This is expected, given the high material losses of the system, and the modest Q value achieved [1]. As a matter of fact these two factors bring us quite far from a possible *thresholdless laser* regime [15].

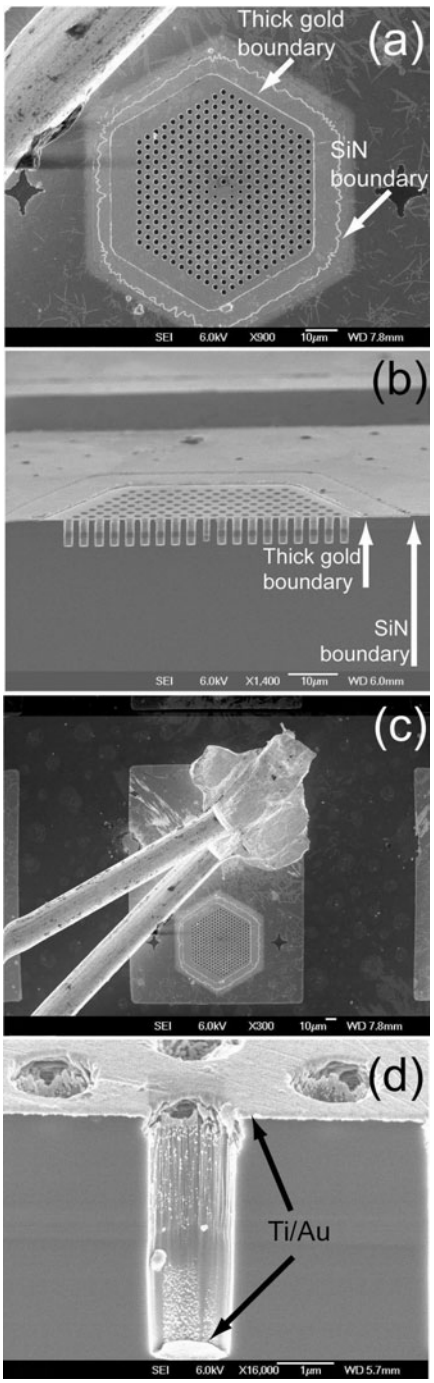

Figure 7. SEM images of a typical complete device. (a) Top-view close-up of the device. The boundary of the window opened in the SiN layer is clearly visible, together with the hexagonal shape of the thick Ti/Au contact (both indicated by arrows). (b) Image of a cleaved device. The same two boundaries as in panel (a) are indicated by the two white arrows. (c) Top-view of a complete device with bonding wires for the injection of current. The size of the rectangular metal pad is 210 × 150 μm. (d) Close-up of a hole of a cleaved typical device, after the second metal evaporation. The metal is clearly deposited on the top surface and on the bottom of the holes (indicated by arrows). On the other hand, very little Ti/Au is deposited on the sidewalls of the hole, thanks to the extreme verticality of the etching.

Figure 9 shows the electroluminescence spectra of typical devices in three different conditions. When the PC resonances

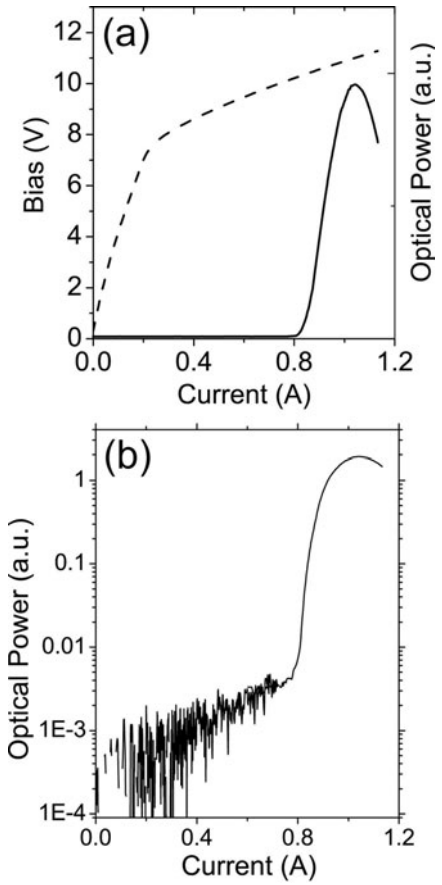

Figure 8. (a) L–V–I characteristic of a typical device at 10 K. (b) L–I of the same device in log-linear scale, clearly showing the presence of the threshold for laser action.

do not overlap the gain spectrum (figure 9(a)), the emission is near-Lorentzian with a full-width at half-maximum (FWHM) of $\sim$100 cm^{-1} centred at the QC heterostructure design wavelength. When the PC resonances overlap with the gain spectrum, a set of three emission peaks (corresponding to the frequency regions of the band-structure in figure 1) emerge on top of the broad EL spectrum (figure 9(b)). The spectral position of these peaks can be tuned as a function of a and r, confirming that they indeed are related to Bragg scattering in the PC microcavity. Finally, the spectrum of a device in lasing mode is shown in figure 9(c).

6. Conclusions and outlook

We have presented the technological methods necessary to fabricate photonic-crystal microcavity quantum cascade lasers. The devices presented in this work combine the advanced electronic band-gap engineering exploited in QC lasers and the optical dispersion engineering of photonic crystals. The combination of miniaturization, vertical emission and lithographic tailorability makes these devices potentially interesting for several trace-gas and spectroscopy applications. Nevertheless, significant engineering issues need to be addressed in order to achieve device performances (laser threshold, operating temperature) comparable to standard QC laser technology. The problems of current spreading and

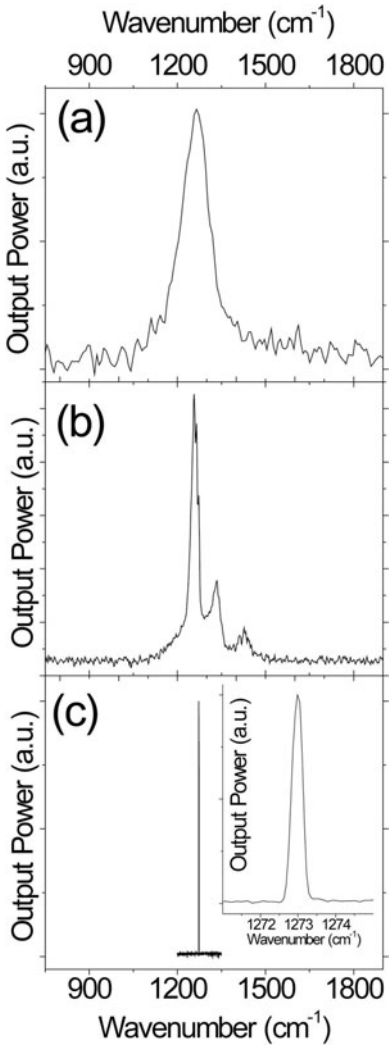

Figure 9. Electro-luminescence spectra for typical PC QC devices in different conditions: when the PC resonances do not overlap the gain spectrum (a) and when they overlap the gain spectrum (b). Panel (c) shows the laser emission just above threshold. The inset of panel (c) is a close-up of the emission, showing the exact emission wavelength.

unwanted metal in the etched holes will be the first to be addressed in future works. The former can be limited through electrical isolation by ion implantation or by etching deep mesas around the PC devices. We in fact estimate that, in these initial devices, current spreading increases the threshold current density by at least a factor of 2. The latter can instead be completely avoided by depositing the top metal contact *prior* to etching the semiconductor layers. Further performances improvements will follow from the optimization of the semiconductor etch. Surface-plasmon waveguides have been used in this initial work because they do not contain AlInAs claddings, whose etching did not result as good as on InGaAs/InP. Unfortunately, surface-plasmon waveguides exhibit very high losses at these wavelengths ($\approx$8 μm). The current devices are therefore penalized by this choice: optimization of AlInAs ICP-etching will allow the use of higher-performance QC material.

Acknowledgments

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