First Experimental Demonstration of Gate-all-around III-V MOSFET by Top-down Approach

The Harvard community has made this article openly available. Please share how this access benefits you. Your story matters

---

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Citable link</td>
<td><a href="http://nrs.harvard.edu/urn-3:HUL.InstRepos:8231688">http://nrs.harvard.edu/urn-3:HUL.InstRepos:8231688</a></td>
</tr>
<tr>
<td>Terms of Use</td>
<td>This article was downloaded from Harvard University’s DASH repository, and is made available under the terms and conditions applicable to Open Access Policy Articles, as set forth at <a href="http://nrs.harvard.edu/urn-3:HUL.InstRepos:dash.current.terms-of-use#OAP">http://nrs.harvard.edu/urn-3:HUL.InstRepos:dash.current.terms-of-use#OAP</a></td>
</tr>
</tbody>
</table>
**First Experimental Demonstration of Gate-all-around III-V MOSFETs by Top-down Approach**

**J.J. Gu,1) Y.Q. Liu,2) Y.Q. Wu,1) R. Colby,1) R.G. Gordon,2) and P. D. Ye1)**

1) School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906, U.S.A.
2) Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.

Tel: 1-765-494-7611, Fax: 1-765-496-7443, Email: yep@purdue.edu

**Introduction:** Recently, continuous progress has been made in the understanding and improvement of high-k/III-V interfaces. However, to realize III-V FETs beyond the 15nm technology node, emerging 3D device structures are necessary to suppress short-channel effects (SCE). III-V FinFETs [1-2] as well as multi-gate quantum-well FETs [3] have been shown to improve greatly the off-state performance of III-V FETs with deep submicron gate lengths. On the other hand, the gate-all-around (GAA) structure has been proven on Si CMOS to be the most resistant to SCE, thanks to having the best gate electrostatic control. Therefore, a III-V GAA FET is the most promising candidate for the ultimate scaling of III-V FETs. In this abstract, we report the first experimental demonstration of inversion-mode \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) GAA FETs by a top-down approach with atomic-layer-deposited (ALD) \( \text{Al}_2\text{O}_3/\text{WN} \) gate stacks. Benefiting from the GAA structure, we have demonstrated the shortest gate length \( (L_G = 50\text{nm}) \) III-V MOSFETs to date with well-behaved on-state and off-state characteristics. A systematic scaling metrics study has been carried out for \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) GAA FETs with \( L_G \) from 110nm down to 50nm, with fin widths \( (W_{\text{Fin}}) \) of 30nm and 50nm, fin height \( (H_{\text{Fin}}) \) of 30nm and wire lengths \( (L_{NW}) = 150 \) to 200nm.

**Experiments:** Fig. 1 shows a schematic view of a \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) GAA FET fabricated in this work. The starting material is 30nm p- \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) on p+ (100) InP substrate. Table 1 and Fig. 2 depict the key fabrication processes for \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) GAA FETs. Fig. 3 (a)-(b) demonstrates the novel InGaAs channel release process and Fig. 3(c) shows the SEM image of a finished device. Devices with different numbers of parallel channels (1 wire, 4 wires, 9 wires or 19 wires) were fabricated in this work. Fig. 4 shows the fin patterning direction (along [010] direction) and device alignment to the substrate for a successful release process.

**Results and discussion:** Fig. 5 - 6 show the well-behaved output and transfer characteristics as well as \( I_g-V_g \) of a \( L_G=50\text{nm} \) GAA FET. The current is normalized by the total perimeter of the \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) channel, i.e. \( W_G = (2W_{\text{Fin}}+2H_{\text{Fin}})\times(\text{No. of wires}). \) A representative 50nm \( L_G \) device shows on-current over 700\( \mu \)A/\( \mu \)m, transconductance over 500\( \mu \)S/\( \mu \)m and reasonable off-state characteristics with subthreshold swing (SS) of 150mV/dec and drain-induced barrier lowering (DIBL) of 210mV. Although operating in inversion-mode, the threshold voltage of the device is -0.68V from linear extrapolation at \( V_{ds}=50\text{mV} \) due to the relatively small work function of ALD WN metal (-4.6eV). Due to the junction leakage current and a very large area ratio (>10\(^4\)) between implanted junction and GAA channels, the source current is used to obtain the intrinsic current in the channel. Gate leakage current is minimal in the entire gate voltage range, indicating 10nm \( \text{Al}_2\text{O}_3 \) is sufficient for GAA structure and further EOT scaling is achievable. Source current saturates at negative \( V_{gs} \) due to a leakage path underneath the bottom gate and limits the on-off ratio of the device. Fig. 7 shows the extrinsic and intrinsic transconductance at \( V_{ds}=1V \) for the same device. The source/drain resistance \( R_{SD} \) is extracted to be around 1150\( \Omega \). The maximum intrinsic transconductance is 750\( \mu \)S/\( \mu \)m. Fig. 8 shows the \( I_{ON} \) and \( g_m \) scaling metrics for \( L_G=50-110\text{nm} \) and \( W_{\text{Fin}}=30\text{nm} \). From Fig. 9, 30nm \( W_{\text{Fin}} \) devices show better \( V_T \) roll-off properties when \( L_G \) is shrinking. The SS for 30nm \( W_{\text{Fin}} \) devices are almost unchanged at around 150mV/dec when scaling \( L_G \) down to 50nm, indicating excellent control of SCE and improved interface property considering the large EOT, whereas the 50nm \( W_{\text{Fin}} \) devices show larger SS, which increases with scaling of \( L_G \). Fig. 11 shows that 30nm \( W_{\text{Fin}} \) devices have smaller DIBL. Further DIBL reduction can be achieved by scaling down EOT. Fig. 12 shows the transfer characteristics for two GAA FETs with 1 wire and 4 wires in parallel, respectively. Fig. 13 – 14 shows a linear relationship of \( I_{max} \) and \( g_m \) with the number of wires in both the linear and saturation regimes. Each wire can deliver a \( I_{sat}=90\mu \)A and \( g_m =66\mu \)A/\( \mu \)m at \( V_{ds}=1V \). Fig. 15 shows the output characteristic for a hero GAA FET with the \( I_{ON}=1.71\text{mA}/\mu \)m. Fig. 16 benchmarks the \( g_m \times EOT \) product vs. \( L_G \) of \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) GAA FETs in this work with surface channel InGaAs MOSFETs [57-10]. Table 2 compares the device structure and performance of \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) GAA FETs in this work with all published non-planar 3D III-V FETs [1-3][7]. Due to the excellent electrostatic control of the channel by GAA structure, \( L_G \) has been pushed down to 50nm with excellent on- and off-state performance.

**Conclusions:** We have demonstrated for the first time inversion-mode \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) GAA MOSFETs with ALD \( \text{Al}_2\text{O}_3/\text{WN} \) gate stacks. The highest saturation current reaches 1.71mA/\( \mu \)m at \( V_{ds}=1V \). The SCE of III-V MOSFETs is greatly improved by the 3D structure design, making III-V GAA FET a very promising candidate for ultimately scaled III-V device technology.

**Acknowledgement:** The authors would like to thank R. Wang, M. Luisier, M. S. Lundstrom, C. Zhang and X. L. Li for valuable discussions and technical assistance. This work is supported by the FCRP MSD Center and NSF.

**References:**

Fig. 1 Schematic view of an inversion-mode GAA n-channel In_{0.53}Ga_{0.47}As (2×10^{19}/cm^2) MOSFET with 10nm ALD Al_{2}O_{3}/20nm WN gate stack. A heavily doped wide bandgap InP lies underneath the channel.

Table 1 Fabrication process flow for inversion-mode high-k/InGaAs GAA FETs. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system. Dry etching was carried out by a Panasonic E620 high density plasma etcher.

Fig. 2 Schematic diagram of key process steps in the fabrication of InGaAs GAA MOSFETs.

Fig. 3 (a) Tilted SEM image of free-standing InGaAs nanowire test structures after the release process. (b) Cross-sectional TEM image of InGaAs nanowire test structures wrapped by 50nm ALD Al_{2}O_{3} on InP substrate, confirming the nanowires are completely released (c) Top view SEM image of a finished InGaAs GAA FET with 4 parallel wires of W_{Fin} = 30nm, L_{NW} = 200nm and L_{G} = 50nm.

Fig. 4 Schematic diagram of fin patterning direction and etching profile.

Fig. 5 Output characteristic of a representative GAA FET with L_{G}=50nm, W_{Fin}=30nm. The current from each wire is normalized by 120nm, the perimeter of the channel.

Fig. 6 Transfer characteristic and gate leakage current of a representative GAA FET with L_{G}=50nm and W_{Fin}=30nm.
Fig. 7 Current and extrinsic/intrinsic transconductance in saturation regime. The source/drain resistance $R_{SD}$ is extracted to be 1150$\Omega \mu$m.

Fig. 8 $I_{ON}$ and $g_m$ vs. $L_G$ for GAA FETs with $W_{Fin}=30$nm. The values are determined by measuring 20 different devices at the same $L_G$. Error bar shows statistical variations of multiple devices.

Fig. 9 $V_{de}$ vs. $L_G$ for GAA FETs with $W_{Fin}=30$nm and 50nm. Smaller $W_{Fin}$ shows better $V_{de}$ roll-off.

Fig. 10 SS vs. $L_G$ for GAA FETs with $W_{Fin}=30$nm and 50nm. The estimated upper limit of midgap $D_a$ from SS is $5.6 \times 10^{12}$ $/cm^2$-$V$, a factor of 2 lower than those reported in [1].

Fig. 11 DIBL vs. $L_G$ for GAA FETs with $W_{Fin}=30$nm and 50nm.

Fig. 12 Transfer characteristic of GAA FETs with 1 and 4 parallel wires.

Fig. 13 Linear and saturation current for GAA FETs with different number of parallel wires.

Fig. 14 Linear and saturation transconductance for GAA FETs with different number of parallel wires.

Fig. 15 Output characteristic of a hero GAA FET with saturation current of 1.17mA/µm.

Table 2 Comparison of InGaAs GAA FETs in this work and recently reported non-planar III-V FETs.